16-bit Proprietary Microcontroller

CMOS

F²MC-16LX MB90590G Series

MB90591G/F591G/594G/F594G/V590G

■ DESCRIPTION

The MB90590G series with two FULL-CAN interfaces and FLASH ROM is especially designed for automotive and industrial applications. Its main features are two on board CAN Interfaces, which conform to V2.0 Part A and Part B, while supporting a very flexible message buffer scheme and so offering more functions than a normal full CAN approach.

The instruction set of F²MC-16LX CPU core inherits an AT architecture of the F²MC* family with additional instruction sets for high-level languages, extended addressing mode, enhanced multiplication/division instructions, and enhanced bit manipulation instructions. The microcontroller has a 32-bit accumulator for processing long word data.

The MB90590/590G series has peripheral resources of 8/10-bit A/D converters, UART (SCI), extended I/O serial interface, 8/16-bit PPG timer, I/O timer (input capture (ICU), output compare (OCU)), stepping motor controller, and sound generator.

* : F²MC is the abbreviation of Fujitsu Flexible Microcontroller.

For the information for microcontroller supports, see the following web site.

http://edevice.fujitsu.com/micom/en-support/

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■ FEATURES

- Clock
  Embedded PLL clock multiplication circuit
  Operating clock (PLL clock) can be selected from divided-by-2 of oscillation or one to four times the oscillation (at oscillation of 4 MHz, 4 MHz to 16 MHz).
  Minimum instruction execution time : 62.5 ns (operation at oscillation of 4 MHz, four times the oscillation clock, V_{CC} of 5.0 V)
- Instruction set to optimize controller applications
  Rich data types (bit, byte, word, long word)
  Rich addressing mode (23 types)
  Enhanced signed multiplication/division instruction and RETI instruction functions
  Enhanced precision calculation realized by the 32-bit accumulator
- Instruction set designed for high level language (C language) and multi-task operations
  Adoption of system stack pointer
  Enhanced pointer indirect instructions
  Barrel shift instructions
- Program patch function (for two address pointers)
- Enhanced execution speed : 4-byte instruction queue
- Enhanced interrupt function : 8 levels, 34 factors
- Automatic data transmission function independent of CPU operation
  Extended intelligent I/O service function (EI²OS) : Up to 10 channels
- Embedded ROM size and types
  Mask ROM : 256 Kbytes/384 Kbytes
  Flash ROM : 256 Kbytes/384 Kbytes
  Embedded RAM size : 6 Kbytes/8 Kbytes
- Flash ROM
  Supports automatic programming, Embedded Algorithm
  Write/Erase/Erase-Suspend/Resume commands
  A flag indicating completion of the algorithm
  Hard-wired reset vector available in order to point to a fixed boot sector in Flash Memory
  Erase can be performed on each block
  Block protection with external programming voltage
- Low-power consumption (stand-by) mode
  Sleep mode (mode in which CPU operating clock is stopped)
  Stop mode (mode in which oscillation is stopped)
  CPU intermittent operation mode
  Watch mode
  Hardware stand-by mode
- Process
  0.5μm CMOS technology
- I/O port
  General-purpose I/O ports : 78 ports
- Timer
  Watchdog timer : 1 channel
  8/16-bit PPG timer : 8/16-bit × 6 channels
  16-bit re-load timer : 2 channels

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- 16-bit I/O timer
  16-bit free-run timer : 1 channel
  Input capture : 6 channels
  Output compare : 6 channels
- Extended I/O serial interface : 1 channel
- UART (3 channels)
  With full-duplex double buffer (8-bit length)
  Clock asynchronized or clock synchronized (with start/stop bit) transmission can be selectively used.
- Stepping motor controller (4 channels)
- External interrupt circuit (8 channels)
  A module for starting an extended intelligent I/O service (EI^{2}OS) and generating an external interrupt which is triggered by an external input.
- Delayed interrupt generation module
  Generates an interrupt request for switching tasks.
- 8/10-bit A/D converter (8 channels)
  8/10-bit resolution can be selectively used.
  Starting by an external trigger input.
- FULL-CAN interfaces : 2
  Conforming to Version 2.0 Part A and Part B
  Flexible message buffering (mailbox and FIFO buffering can be mixed)
- Sound generator
- 18-bit Time-base counter
- Watch timer : 1 channel
- External bus interface : Maximum address space 16 Mbytes

■ PRODUCT LINEUP

Features		MB90591G/594G	MB90F591G/F594G	MB90V590G
Classification		Mask ROM product	Flash ROM product	Evaluation product
ROM size		384/256 Kbytes	384/256 Kbytes Boot block Hard-wired reset vector	None
RAM size		8/6 Kbytes	8/6 Kbytes	8 Kbytes
Emulator-specific power supply *1		—		None
CPU functions		The number of instructions : 340 Instruction bit length : 8 bits, 16 bits Instruction length : 1 byte to 7 bytes Data bit length : 1 bit, 8 bits, 16 bits Minimum execution time : 62.5 ns (at machine clock frequency of 16 MHz) Interrupt processing time : 1.5 μs (at machine clock frequency of 16 MHz, minimum value)		
UART (3 channels)		Clock synchronized transmission (500 Kbps / 1 Mbps / 2 Mbps) Clock asynchronized transmission (4808/5208/9615/10417/19230/38460/62500 /500000 bps at machine clock frequency of 16 MHz) Transmission can be performed by bi-directional serial transmission or by master/slave connection.		
8/10-bit A/D converter		Conversion precision : 8/10-bit can be selectively used. Number of inputs : 8 One-shot conversion mode (converts selected channel once only) Scan conversion mode (converts two or more successive channels and can program up to 8 channels) Continuous conversion mode (converts selected channel continuously) Stop conversion mode (converts selected channel and stop operation repeatedly)		
8/16-bit PPG timers (6 channels)		Number of channels : 6 (8/16-bit $\times$ 6 channels) PPG operation of 8-bit or 16-bit A pulse wave of given intervals and given duty ratios can be output. Pulse interval : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4, 128μs (at oscillation of 4 MHz, fsys = system clock frequency of 16 MHz, fosc = oscillation clock frequency)		
16-bit Reload timer		Number of channels : 2 Operation clock frequency : fsys/2^1, fsys/2^3, fsys/2^5 (fsys = System clock frequency) Supports External Event Count function		
16-bit I/O timer	16-bit Output compares	Number of channels : 6 (8/16-bit $\times$ 6 channels) Pin input factor : A match signal of compare register		
	Input captures	Number of channels : 6 Rewriting a register value upon a pin input (rising, falling, or both edges)		

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| Features	MB90591G/594G	MB90F591G/F594G	MB90V590G
CAN Interface	Number of channels : 2 Conforms to CAN Specification Version 2.0 Part A and B Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 message buffers for data and ID's Supports multiple messages Flexible configuration of acceptance filtering : Full bit compare / Full bit mask / Two partial bit masks Supports up to 1Mbps CAN bit timing setting : MB90(F)59xG : TSEG2 $\geq$ RSJW		
Stepping motor controller (4 channels)	Four high current outputs for each channel Synchronized two 8-bit PWM's for each channel		
External interrupt circuit	Number of inputs : 8 Started by a rising edge, a falling edge, an "H" level input, or an "L" level input.		
Sound generator	8-bit PWM signal is mixed with tone frequency from 8-bit reload counter PWM frequency : 62.5K, 31.2K, 15.6K, 7.8KHz (at System clock = 16MHz) Tone frequency : PWM frequency / 2 / (reload value + 1)		
Extended I/O serial interface	Clock synchronized transmission (31.25K/62.5K/125K/500K/1Mbps at machine clock frequency of 16 MHz) LSB first/MSB first		
Watch timer	Directly operates with the system clock Read/Write accessible Second/Minute/Hour registers		
Watchdog timer	Reset generation interval : 3.58 ms, 14.33 ms, 57.23 ms, 458.75 ms (at oscillation of 4 MHz, minimum value)		
Flash Memory	Supports automatic programming, Embedded Algorithm and Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Hard-wired reset vector available in order to point to a fixed boot sector in Flash Memory Boot block configuration Erase can be performed on each block Block protection with external programming voltage Flash Writer from Minato Electronics Inc.		
Low-power consumption (stand-by) mode	Sleep/stop/CPU intermittent operation/watch timer/hardware stand-by		
Process	CMOS		
Power supply voltage for operation*[2]	5 V$\pm$10 % (MB90V590G, MB90F594G, MB90594G) 5 V$\pm$5 % (MB90F591G, MB90591G)		
Package	QFP-100		PGA-256

*1 : It is setting of DIP switch S2 when Emulation pod (MB2145-507) is used.
    Please refer to the MB2145-507 hardware manual (2.7 Emulator-specific Power Pin) about details.

*2 : Varies with conditions such as the operating frequency. (See section "■ Electrical Characteristics.")

■ PIN ASSIGNMENT

(Top view)

Top pins (left to right, 100–81):
P17/SGA (100), P16/SGO (99), P15/TX1 (98), P14/RX1 (97), P13/OUT5 (96), P12/OUT4 (95), P11/OUT3 (94), P10/OUT2 (93), P07/OUT1 (92), P06/OUT0 (91), P05/IN5 (90), P04/IN4 (89), P03/IN3 (88), P02/IN2 (87), P01/IN1 (86), P00/IN0 (85), Vcc (84), X1 (83), X0 (82), Vss (81)

Left pins (top to bottom, 1–30):
Pin	Signal
1	P20
2	P21
3	P22
4	P23
5	P24/INT4
6	P25/INT5
7	P26/INT6
8	P27/INT7
9	P30
10	P31
11	Vss
12	P32
13	P33
14	P34/SOT0
15	P35/SCK0
16	P36/SIN0
17	P37/SIN1
18	P40/SCK1
19	P41/SOT1
20	P42/SOT2
21	P43/SCK2
22	P44/SIN2
23	Vcc
24	P45/SCIN3
25	P46/SCK3
26	P47/SOT3
27	C
28	P50/PPG0
29	P51/PPG1
30	P52/PPG2

Right pins (top to bottom, 80–51):
Pin	Signal
80	P95/INT3
79	P94/INT2
78	P93/INT1
77	$\overline{RST}$
76	P92/INT0
75	P91/RX0
74	P90/TX0
73	DVss
72	P87/PWM2M3
71	P86/PWM2P3
70	P85/PWM1M3
69	P84/PWM1P3
68	DVcc
67	P83/PWM2M2
66	P82/PWM2P2
65	P81/PWM1M2
64	P80/PWM1P2
63	DVss
62	P77/PWM2M1
61	P76/PWM2P1
60	P75/PWM1M1
59	P74/PWM1P1
58	DVcc
57	P73/PWM2M0
56	P72/PWM2P0
55	P71/PWM1M0
54	P70/PWM1P0
53	DVss
52	$\overline{HST}$
51	MD2

Bottom pins (left to right, 31–50):
P53/PPG3 (31), P54/PPG4 (32), P55/PPG5/ADTG (33), AVcc (34), AVRH (35), AVRL (36), AVss (37), P60/AN0 (38), P61/AN1 (39), P62/AN2 (40), P63/AN3 (41), Vss (42), P64/AN4 (43), P65/AN5 (44), P66/AN6 (45), P67/AN7 (46), P56/TIN (47), P57/TOT/WOT (48), MD0 (49), MD1 (50)

(FPT-100P-M06)

■ PIN DESCRIPTION

No.	Pin name	Circuit type	Function
82	X0	A	Oscillator pin
83	X1		
77	$\overline{RST}$	B	Reset input
52	$\overline{HST}$	C	Hardware standby input
85 to 90	P00 to P05	D	General purpose I/O
	IN0 to IN5		Inputs for the Input Captures
91 to 96	P06, P07, P10 to P13	D	General purpose I/O
	OUT0 to OUT5		Outputs for the Output Compares. To enable the signal outputs, the corresponding bits of the Port Direction registers should be set to "1".
97	P14	D	General purpose I/O
	RX1		RX input for CAN Interface 1
98	P15	D	General purpose I/O
	TX1		TX output for CAN Interface 1. To enable the signal output, the corresponding bit of the Port Direction register should be set to "1".
99	P16	D	General purpose I/O
	SGO		SGO output for the Sound Generator. To enable the signal output, the corresponding bit of the Port Direction register should be set to "1".
100	P17	D	General purpose I/O
	SGA		SGA output for the Sound Generator. To enable the signal output, the corresponding bit of the Port Direction register should be set to "1".
1 to 4	P20 to P23	D	General purpose I/O
5 to 8	P24 to P27	D	General purpose I/O
	INT4 to INT7		External interrupt input for INT4 to INT7
9, 10	P30, P31	D	General purpose I/O
12, 13	P32, P33	D	General purpose I/O
14	P34	D	General purpose I/O
	SOT0		SOT output for UART 0. To enable the signal output, the corresponding bit of the Port Direction register should be set to "1".
15	P35	D	General purpose I/O
	SCK0		SCK input/output for UART 0. To enable the signal output, the corresponding bit of the Port Direction register should be set to "1".

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No.	Pin name	Circuit type	Function
16	P36	D	General purpose I/O
	SIN0		SIN input for UART 0
17	P37	D	General purpose I/O
	SIN1		SIN input for UART 1
18	P40	D	General purpose I/O
	SCK1		SCK input/output for UART 1
19	P41	D	General purpose I/O
	SOT1		SOT output for UART 1
20	P42	D	General purpose I/O
	SOT2		SOT output for UART 2
21	P43	D	General purpose I/O
	SCK2		SCK input/output for UART 2
22	P44	D	General purpose I/O
	SIN2		SIN input for UART 2
24	P45	D	General purpose I/O
	SIN3		SIN input for the Serial I/O
25	P46	D	General purpose I/O
	SCK3		SCK input/output for the Serial I/O
26	P47	D	General purpose I/O
	SOT3		SOT output for the Serial I/O
28 to 33	P50 to P55	D	General purpose I/O
	PPG0 to PPG5, ADTG		Outputs for the Programmable Pulse Generators. Pin number 33 is also shared with ADTG input for the external trigger of the A/D Converter.
38 to 41	P60 to P63	E	General purpose I/O
	AN0 to AN3		Inputs for the A/D Converter
43 to 46	P64 to P67	E	General purpose I/O
	AN4 to AN7		Inputs for the A/D Converter
47	P56	D	General purpose I/O
	TIN		TIN input for the 16-bit Reload Timers
48	P57	D	General purpose I/O
	TOT/WOT		TOT output for the 16-bit Reload Timers and WOT output for the Watch Timer. Only one of three output enable flags in these peripheral blocks can be set at a time. Otherwise the output signal has no meaning.

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No.	Pin name	Circuit type	Function
54 to 57	P70 to P73	F	General purpose I/O
	PWM1P0, PWM1M0, PWM2P0, PWM2M0		Output for Stepping Motor Controller channel 0.
59 to 62	P74 to P77	F	General purpose I/O
	PWM1P1, PWM1M1, PWM2P1, PWM2M1		Output for Stepping Motor Controller channel 1.
64 to 67	P80 to P83	F	General purpose I/O
	PWM1P2, PWM1M2, PWM2P2, PWM2M2		Output for Stepping Motor Controller channel 2.
69 to 72	P84 to P87	F	General purpose I/O
	PWM1P3, PWM1M3, PWM2P3, PWM2M3		Output for Stepping Motor Controller channel 3.
74	P90	D	General purpose I/O
	TX0		TX output for CAN Interface 0
75	P91	D	General purpose I/O
	RX0		RX input for CAN Interface 0
76	P92	D	General purpose I/O
	INT0		External interrupt input for INT0
78	P93	D	General purpose I/O
	INT1		External interrupt input for INT1
79	P94	D	General purpose I/O
	INT2		External interrupt input for INT2
80	P95	D	General purpose I/O
	INT3		External interrupt input for INT3
58, 68	DV$_{CC}$	—	Dedicated power supply pins for the high current output buffers (Pin No. 54 to 72)
53, 63, 73	DV$_{SS}$	—	Dedicated ground pins for the high current output buffers (Pin No. 54 to 72)
34	AV$_{CC}$	Power supply	Power supply for analog circuit pin. When turning this power supply on or off, always be sure to first apply electric potential equal to or greater than AV$_{CC}$ to V$_{CC}$.
37	AV$_{SS}$	Power supply	Ground level for analog circuit

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No.	Pin name	Circuit type	Function
35	AVRH	Power supply	Reference voltage input pin for analog circuit When turning this power supply on or off, always be sure to first apply electric potential equal to or greater than AVRH to AV_{CC}.
36	AVRL	Power supply	Reference voltage input pin for analog circuit
49, 50	MD0, MD1	C	Operating mode selection input pins Connect directly to V_{CC} or V_{SS}.
51	MD2	G	Operating mode selection input pin Connect directly to V_{CC} or V_{SS}.
27	C	—	This is the power supply stabilization capacitor pin. It should be connected externally to an 0.1 μF ceramic capacitor.
23, 84	V_{CC}	Power supply	Power supply (5.0 V) input pin for digital circuit
11,42,81	V_{SS}	Power supply	Power supply (GND) input pin for digital circuit

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■ I/O CIRCUIT TYPE

Circuit Type	Circuit	Remarks
A		• Oscillation feedback resistor : 1 MΩ approx.
B		• Hysteresis input with pull-up resistor : 50 kΩ approx.
C		• Hysteresis input
D		• CMOS output • Hysteresis input
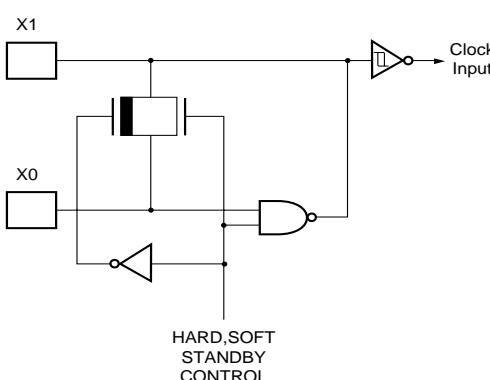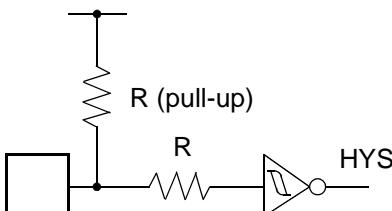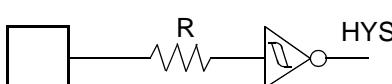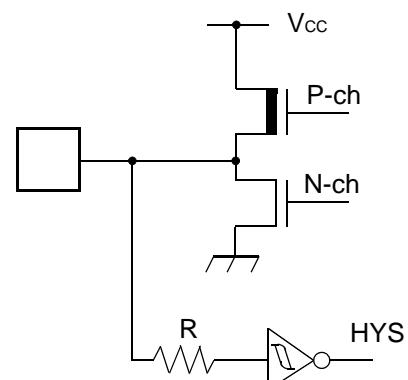
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Circuit Type	Circuit	Remarks
E		• CMOS output • Hysteresis input • Analog input
F		• CMOS high current output • Hysteresis input
G		• Hysteresis input with pull-down resistor : 50 kΩ approx. • Flash version does not have pull-down resistor.

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■ HANDLING DEVICES

(1) Preventing latch-up

CMOS IC chips may suffer latch-up under the following conditions :
• A voltage higher than Vcc or lower than Vss is applied to an input or output pin.
• A voltage higher than the rated voltage is applied between Vcc and Vss.
• The AVcc power supply is applied before the Vcc voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

For the same reason, also be careful not to let the analog power-supply voltage (AV$_{CC}$, AVRH) exceed the digital power-supply voltage.

(2) Treatment of unused pins

Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefor they must be pulled up or pulled down through resistors. In this case those resistors should be more than 2 kΩ.
Unused bidirectional pins should be set to the output state and can be left open, or the input state with the above described connection.

(3) Using external clock

To use external clock, drive X0 pin only and leave X1 pin unconnected.

Below is a diagram of how to use external clock.
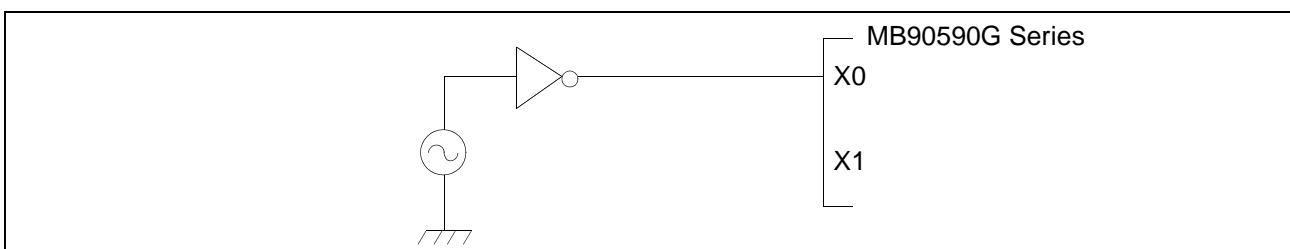

Using external clock

(4)Power supply pins (Vcc/Vss)

In products with multiple V_{CC} or V_{SS} pins, pins with the same potential are internally connected in the device to avoid abnormal operations including latch-up. However, you must connect the pins to an external power and a ground line to lower the electro-magnetic emission level to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total current rating.
Make sure to connect V_{CC} and V_{SS} pins via lowest impedance to power lines.
It is recommended to provide a bypass capacitor of around 0.1 μF between V_{CC} and V_{SS} pin near the device.
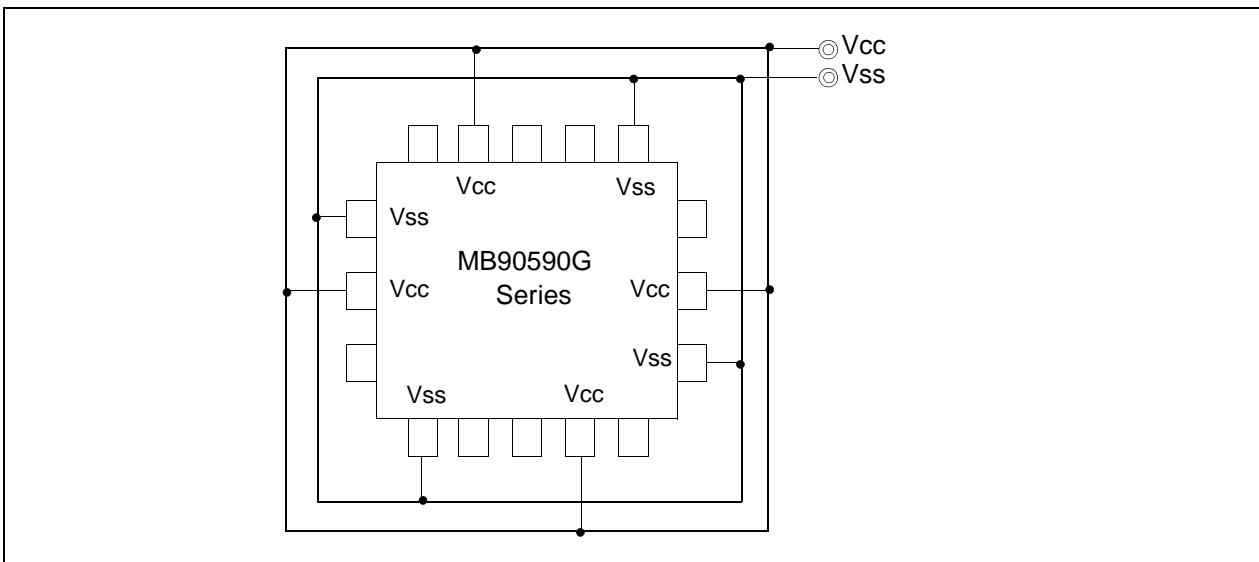
(5) Pull-up/down resistors

The MB90590G Series does not support internal pull-up/down resistors. Use external components where needed.

(6) Crystal Oscillator Circuit

Noises around X0 or X1 pins may cause abnormal operations. Make sure to provide bypass capacitors via the shortest distances from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure that lines of oscillation circuits do not cross the lines of other circuits.

A printed circuit board artwork surrounding the X0 and X1 pins with a ground area for stabilizing the operation is highly recommended.

(7) Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply (AV_{CC}, AVRH, AVRL) and analog inputs (AN0 to AN7) after turning-on the digital power supply (V_{CC}).

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage does not exceed AVRH or AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable).

(8) Connection of Unused Pins of A/D Converter

Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = V_{SS}$.

(9) N.C. Pin

The N.C. (internally connected) pin must be opened for use.

(10) Notes on Energization

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 μs or more (0.2 V to 2.7 V).

(11) Indeterminate outputs from ports 0 and 1 (without MB90F591G/591G, MB90F594G)

During oscillation setting time of step-down circuit (during a power-on reset) after the power is turned on, the outputs from ports 0 and 1 become following state.
- If $\overline{RST}$ pin is "H", the outputs become indeterminate.
- If $\overline{RST}$ pin is "L", the outputs become high-impedance.

Pay attention to the port output timing shown as follow.

$\overline{RST}$ pin is "H"

Oscillation setting time[*2]

Power-on reset[*1]

Vcc (Power-supply pin)
PONR (power-on reset) signal
$\overline{RST}$ (external asynchronous reset) signal
RST (internal reset) signal
Oscillation clock signal
KA (internal operation clock A) signal
KB (internal operation clock B) signal
PORT (port output) signal

Period of indeterminated

*1 : Power-on reset time : "Period of clock frequency" × 2^{17} (Clock frequency of 16 MHz : 8.19 ms)
*2 : Oscillation setting time : "Period of clock frequency" × 2^{18} (Clock frequency of 16 MHz : 16.38ms)

$\overline{RST}$ pin is "L"

Oscillation setting time[*2]

Power-on reset[*1]

Vcc (Power-supply pin)
PONR (power-on reset) signal
$\overline{RST}$ (external asynchronous reset) signal
RST (internal reset) signal
Oscillation clock signal
KA (internal operation clock A) signal
KB (internal operation clock B) signal
PORT (port output) signal

High-impedance

*1 : Power-on reset time : "Period of clock frequency" × 2^{17} (Clock frequency of 16 MHz : 8.19 ms)
*2 : Oscillation setting time : "Period of clock frequency" × 2^{18} (Clock frequency of 16 MHz : 16.38ms)

(12) Initialization

The device contains internal registers which are initialized only by a power-on reset. To initialize these registers, please turn on the power again.

(13) Directions of "DIV A, Ri" and "DIVW A, RWi" instructions

In the Signed multiplication and division instructions ("DIV A, Ri" and "DIVW A, RWi"), the value of the corresponding bank register (DTB, ADB, USB, SSB) is set in "00 $_H$".

If the values of the corresponding bank registers (DTB,ADB,USB,SSB) are set to other than "00 $_H$", the remainder by the execution result of the instruction is not stored in the register of the instruction operand.

(14) Using REALOS

The use of EI^{2}OS is not possible with the REALOS real time operating system.

(15) Caution on Operations during PLL Clock Mode

If the PLL clock mode is selected in the microcontroller, it may attempt to continue the operation using the free-running frequency of the automatic oscillating circuit in the PLL circuitry even if the oscillator is out of place or the clock input is stopped. Performance of this operation, however, cannot be guaranteed.

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■ **BLOCK DIAGRAM**
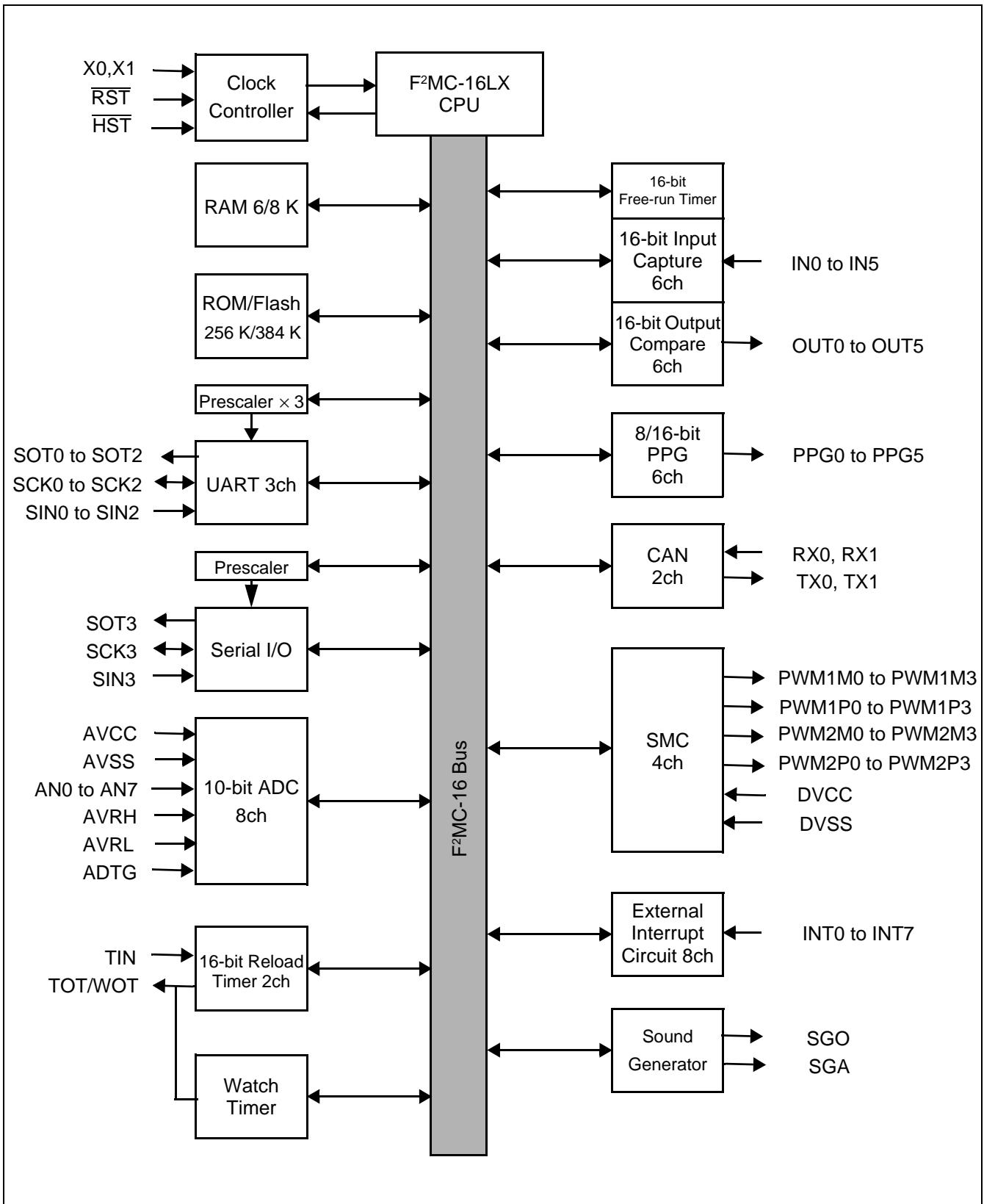
■ MEMORY SPACE

The memory space of the MB90590/590G Series is shown below

MB90V590G

Address	Region
FFFFFF$_H$ / FF0000$_H$	ROM (FF bank)
FEFFFF$_H$ / FE0000$_H$	ROM (FE bank)
FDFFFF$_H$ / FD0000$_H$	ROM (FD bank)
FCFFFF$_H$ / FC0000$_H$	ROM (FC bank)
FBFFFF$_H$ / FB0000$_H$	ROM (FB bank)
FAFFFF$_H$ / FA0000$_H$	ROM (FA bank)
F9FFFF$_H$ / F90000$_H$	ROM (F9 bank)
00FFFF$_H$ / 004000$_H$	ROM (Image of FF bank)
0028FF$_H$ / 002100$_H$ / 0020FF$_H$	RAM 2K
001FFF$_H$ / 001900$_H$ / 0018FF$_H$	Peripheral
000100$_H$	RAM 6K
0000BF$_H$ / 000000$_H$	Peripheral

MB90594G/F594G

Address	Region
FFFFFF$_H$ / FF0000$_H$	ROM (FF bank)
FEFFFF$_H$ / FE0000$_H$	ROM (FE bank)
FDFFFF$_H$ / FD0000$_H$	ROM (FD bank)
FCFFFF$_H$ / FC0000$_H$	ROM (FC bank)
00FFFF$_H$ / 004000$_H$	ROM (Image of FF bank)
001FFF$_H$ / 001900$_H$ / 0018FF$_H$	Peripheral
000100$_H$	RAM 6K
0000BF$_H$ / 000000$_H$	Peripheral

MB90591G/ F591G

Address	Region
FFFFFF$_H$ / FF0000$_H$	ROM (FF bank)
FEFFFF$_H$ / FE0000$_H$	ROM (FE bank)
FDFFFF$_H$ / FD0000$_H$	ROM (FD bank)
FCFFFF$_H$ / FC0000$_H$	
FBFFFF$_H$ / FB0000$_H$	ROM (FB bank)
FAFFFF$_H$ / FA0000$_H$	ROM (FA bank)
F9FFFF$_H$ / F90000$_H$	ROM (F9 bank)
00FFFF$_H$ / 004000$_H$	ROM (Image of FF bank)
0028FF$_H$ / 002100$_H$ / 0020FF$_H$	RAM 2K
001FFF$_H$ / 001900$_H$ / 0018FF$_H$	Peripheral
000100$_H$	RAM 6K
0000BF$_H$ / 000000$_H$	Peripheral

Memory space map

Note : The ROM data of bank FF is reflected in the upper address of bank 00, realizing effective use of the C compiler small model. The lower 16-bit of bank FF and the lower 16-bit of bank 00 are assigned to the same address, enabling reference of the table on the ROM without stating "far".
For example, if an attempt has been made to access 00C000$_H$, the contents of the ROM at FFC000$_H$ are accessed. Since the ROM area of the FF bank exceeds 48 Kbytes, the whole area cannot be reflected in the image for the 00 bank. The ROM data at FF4000$_H$ to FFFFFF$_H$ looks, therefore, as if it were the image for 004000$_H$ to 00FFFF$_H$. Thus, it is recommended that the ROM data table be stored in the area of FF4000$_H$ to FFFFFF$_H$.

■ I/O MAP

Address	Register	Abbreviation	Access	Peripheral	Initial value
00$_H$	Port 0 Data Register	PDR0	R/W	Port 0	XXXXXXXX$_B$
01$_H$	Port 1 Data Register	PDR1	R/W	Port 1	XXXXXXXX$_B$
02$_H$	Port 2 Data Register	PDR2	R/W	Port 2	XXXXXXXX$_B$
03$_H$	Port 3 Data Register	PDR3	R/W	Port 3	XXXXXXXX$_B$
04$_H$	Port 4 Data Register	PDR4	R/W	Port 4	XXXXXXXX$_B$
05$_H$	Port 5 Data Register	PDR5	R/W	Port 5	XXXXXXXX$_B$
06$_H$	Port 6 Data Register	PDR6	R/W	Port 6	XXXXXXXX$_B$
07$_H$	Port 7 Data Register	PDR7	R/W	Port 7	XXXXXXXX$_B$
08$_H$	Port 8 Data Register	PDR8	R/W	Port 8	XXXXXXXX$_B$
09$_H$	Port 9 Data Register	PDR9	R/W	Port 9	_ _ XXXXXX$_B$
0A$_H$ to 0F$_H$	Reserved				
10$_H$	Port 0 Direction Register	DDR0	R/W	Port 0	0 0 0 0 0 0 0 0$_B$
11$_H$	Port 1 Direction Register	DDR1	R/W	Port 1	0 0 0 0 0 0 0 0$_B$
12$_H$	Port 2 Direction Register	DDR2	R/W	Port 2	0 0 0 0 0 0 0 0$_B$
13$_H$	Port 3 Direction Register	DDR3	R/W	Port 3	0 0 0 0 0 0 0 0$_B$
14$_H$	Port 4 Direction Register	DDR4	R/W	Port 4	0 0 0 0 0 0 0 0$_B$
15$_H$	Port 5 Direction Register	DDR5	R/W	Port 5	0 0 0 0 0 0 0 0$_B$
16$_H$	Port 6 Direction Register	DDR6	R/W	Port 6	0 0 0 0 0 0 0 0$_B$
17$_H$	Port 7 Direction Register	DDR7	R/W	Port 7	0 0 0 0 0 0 0 0$_B$
18$_H$	Port 8 Direction Register	DDR8	R/W	Port 8	0 0 0 0 0 0 0 0$_B$
19$_H$	Port 9 Direction Register	DDR9	R/W	Port 9	_ _ 0 0 0 0 0 0$_B$
1A$_H$	Reserved				
1B$_H$	Analog Input Enable Register	ADER	R/W	Port 6, A/D	1 1 1 1 1 1 1 1$_B$
1C$_H$ to 1F$_H$	Reserved				
20$_H$	Serial Mode Control Register 0	UMC0	R/W	UART0	0 0 0 0 0 1 0 0$_B$
21$_H$	Serial Status Register 0	USR0	R/W		0 0 0 1 0 0 0 0$_B$
22$_H$	Serial Input/Output Data Register 0	UIDR0/ UODR0	R/W		XXXXXXXX$_B$
23$_H$	Rate and Data Register 0	URD0	R/W		0 0 0 0 0 0 0 X$_B$
24$_H$	Serial Mode Control Register 1	UMC1	R/W	UART1	0 0 0 0 0 1 0 0$_B$
25$_H$	Serial Status Register 1	USR1	R/W		0 0 0 1 0 0 0 0$_B$
26$_H$	Serial Input/Output Data Register 1	UIDR1/ UODR1	R/W		XXXXXXXX$_B$
27$_H$	Rate and Data Register 1	URD1	R/W		0 0 0 0 0 0 0 X$_B$

(Continued)

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Address	Register	Abbreviation	Access	Peripheral	Initial value
28$_H$	Serial Mode Control Register 2	UMC2	R/W	UART2	0 0 0 0 0 1 0 0$_B$
29$_H$	Serial Status Register 2	USR2	R/W		0 0 0 1 0 0 0 0$_B$
2A$_H$	Serial Input/Output Data Register 2	UIDR2/ UODR2	R/W		XXXXXXXX$_B$
2B$_H$	Rate and Data Register 2	URD2	R/W		0 0 0 0 0 0 0X$_B$
2C$_H$	Serial Mode Control Register (low-order)	SMCS	R/W	Serial I/O	_ _ _ _0 0 0 0$_B$
2D$_H$	Serial Mode Control Register (high-order)	SMCS	R/W		0 0 0 0 0 0 1 0$_B$
2E$_H$	Serial Data Register	SDR	R/W		XXXXXXXX$_B$
2F$_H$	Edge Selector Register	SES	R/W		_ _ _ _ _ _ _0$_B$
30$_H$	External Interrupt Enable Register	ENIR	R/W	External Interrupt	0 0 0 0 0 0 0 0$_B$
31$_H$	External Interrupt Request Register	EIRR	R/W		XXXXXXXX$_B$
32$_H$	External Interrupt Level Register	ELVR	R/W		0 0 0 0 0 0 0 0$_B$
33$_H$	External Interrupt Level Register	ELVR	R/W		0 0 0 0 0 0 0 0$_B$
34$_H$	A/D Control Status Register 0	ADCS0	R/W	A/D Converter	0 0 0 0 0 0 0 0$_B$
35$_H$	A/D Control Status Register 1	ADCS1	R/W		0 0 0 0 0 0 0 0$_B$
36$_H$	A/D Data Register 0	ADCR0	R		XXXXXXXX$_B$
37$_H$	A/D Data Register 1	ADCR1	R/W		0 0 0 0 1 0 XX$_B$
38$_H$	PPG0 Operation Mode Control Register	PPGC0	R/W	16-bit Programmable Pulse Generator 0/1	0 _ 0 0 0 _ _ 1$_B$
39$_H$	PPG1 Operation Mode Control Register	PPGC1	R/W		0 _ 0 0 0 0 0 1$_B$
3A$_H$	PPG0,1 Output Pin Control Register	PPG01	R/W		0 0 0 0 0 0 0 0$_B$
3B$_H$	Reserved				
3C$_H$	PPG2 Operation Mode Control Register	PPGC2	R/W	16-bit Programmable Pulse Generator 2/3	0 _ 0 0 0 _ _1$_B$
3D$_H$	PPG3 Operation Mode Control Register	PPGC3	R/W		0 _ 0 0 0 0 0 1$_B$
3E$_H$	PPG2,3 Output Pin Control Register	PPG23	R/W		0 0 0 0 0 0 0 0$_B$
3F$_H$	Reserved				
40$_H$	PPG4 Operation Mode Control Register	PPGC4	R/W	16-bit Programmable Pulse Generator 4/5	0 _ 0 0 0 _ _ 1$_B$
41$_H$	PPG5 Operation Mode Control Register	PPGC5	R/W		0 _ 0 0 0 0 0 1$_B$
42$_H$	PPG4,5 Output Pin Control Register	PPG45	R/W		0 0 0 0 0 0 0 0$_B$
43$_H$	Reserved				
44$_H$	PPG6 Operation Mode Control Register	PPGC6	R/W	16-bit Programmable Pulse Generator 6/7	0 _ 0 0 0 _ _ 1$_B$
45$_H$	PPG7 Operation Mode Control Register	PPGC7	R/W		0 _ 0 0 0 0 0 1$_B$
46$_H$	PPG6,7 Output Pin Control Register	PPG67	R/W		0 0 0 0 0 0 0 0$_B$
47$_H$	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
48$_H$	PPG8 Operation Mode Control Register	PPGC8	R/W	16-bit Programmable Pulse Generator 8/9	0 _ 0 0 0 _ _ 1$_B$
49$_H$	PPG9 Operation Mode Control Register	PPGC9	R/W		0 _ 0 0 0 0 0 1$_B$
4A$_H$	PPG8,9 Output Pin Control Register	PPG89	R/W		0 0 0 0 0 0 0 0$_B$
4B$_H$	Reserved				
4C$_H$	PPGA Operation Mode Control Register	PPGCA	R/W	16-bit Programmable Pulse Generator A/B	0 _ 0 0 0 _ _ 1$_B$
4D$_H$	PPGB Operation Mode Control Register	PPGCB	R/W		0 _ 0 0 0 0 1$_B$
4E$_H$	PPGA,B Output Pin Control Register	PPGAB	R/W		0 0 0 0 0 0 0 0$_B$
4F$_H$	Reserved				
50$_H$	Timer Control Status Register 0 (low-order)	TMCSR0	R/W	16-bit Reload Timer 0	0 0 0 0 0 0 0 0$_B$
51$_H$	Timer Control Status Register 0 (high-order)	TMCSR0	R/W		_ _ _ _ 0 0 0 0$_B$
52$_H$	Timer Control Status Register 1 (low-order)	TMCSR1	R/W	16-bit Reload Timer 1	0 0 0 0 0 0 0 0$_B$
53$_H$	Timer Control Status Register 1 (high-order)	TMCSR1	R/W		_ _ _ _ 0 0 0 0$_B$
54$_H$	Input Capture Control Status Register 0/1	ICS01	R/W	Input Capture 0/1	0 0 0 0 0 0 0 0$_B$
55$_H$	Input Capture Control Status Register 2/3	ICS23	R/W	Input Capture 2/3	0 0 0 0 0 0 0 0$_B$
56$_H$	Input Capture Control Status Register 4/5	ICS45	R/W	Input Capture 4/5	0 0 0 0 0 0 0 0$_B$
57$_H$	Reserved				
58$_H$	Output Compare Control Status Register 0	OCS0	R/W	Output Compare 0/1	0 0 0 0 _ _ 0 0$_B$
59$_H$	Output Compare Control Status Register 1	OCS1	R/W		_ _ _0 0 0 0 0$_B$
5A$_H$	Output Compare Control Status Register 2	OCS2	R/W	Output Compare 2/3	0 0 0 0 _ _ 0 0$_B$
5B$_H$	Output Compare Control Status Register 3	OCS3	R/W		_ _ _ 0 0 0 0 0$_B$
5C$_H$	Output Compare Control Status Register 4	OCS4	R/W	Output Compare 4/5	0 0 0 0 _ _ 0 0$_B$
5D$_H$	Output Compare Control Status Register 5	OCS5	R/W		_ _ _ 0 0 0 0 0$_B$
5E$_H$	Sound Control Register (low-order)	SGCR	R/W	Sound Generator	0 0 0 0 0 0 0 0$_B$
5F$_H$	Sound Control Register (high-order)	SGCR	R/W		0 _ _ _ _ _ _ 0$_B$

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
60$_H$	Watch Timer Control Register (low-order)	WTCR	R/W	Watch Timer	0 0 0 _ _ 0 0 0$_B$
61$_H$	Watch Timer Control Register (high-order)	WTCR	R/W		0 0 0 0 0 0 0 0$_B$
62$_H$	PWM Control Register 0	PWC0	R/W	Stepping Motor Controller 0	0 0 0 0 0 _ _ 0$_B$
63$_H$	Reserved				
64$_H$	PWM Control Register 1	PWC1	R/W	Stepping Motor Controller 1	0 0 0 0 0 _ _ 0$_B$
65$_H$	Reserved				
66$_H$	PWM Control Register 2	PWC2	R/W	Stepping Motor Controller 2	0 0 0 0 0 _ _ 0$_B$
67$_H$	Reserved				
68$_H$	PWM Control Register 3	PWC3	R/W	Stepping Motor Controller 3	0 0 0 0 0 _ _ 0$_B$
69$_H$ to 6C$_H$	Reserved				
6D$_H$	Serial I/O Prescaler Register	CDCR	R/W	Prescaler (Serial I/O)	0 XXX 1 1 1 1$_B$
6E$_H$	Timer Control Status Register	TCCS	R/W	16-bit Free-run Timer	0 0 0 0 0 0 0 0$_B$
6F$_H$	ROM Mirror Function Select Register	ROMM	W	ROM Mirror	XXXXXXX1$_B$
70$_H$ to 8F$_H$	Reserved for CAN Interface 0/1. Refer to section about CAN Controller				
90$_H$ to 9D$_H$	Reserved				
9E$_H$	Program Address Detection Control Status Register	PACSR	R/W	Address Match Detection Function	0 0 0 0 0 0 0 0$_B$
9F$_H$	Delayed Interrupt/Release Register	DIRR	R/W	Delayed Interrupt	_ _ _ _ _ _ _ 0$_B$
A0$_H$	Low Power Mode Control Register	LPMCR	R/W	Low Power Controller	0 0 0 1 1 0 0 0$_B$
A1$_H$	Clock Selection Register	CKSCR	R/W	Low Power Controller	1 1 1 1 1 1 0 0$_B$
A2$_H$ to A7$_H$	Reserved				
A8$_H$	Watchdog Timer Control Register	WDTC	R/W	Watchdog Timer	XXXXX 1 1 1$_B$
A9$_H$	Time Base Timer Control Register	TBTC	R/W	Time Base Timer	1 - - 0 0 1 0 0$_B$
AA$_H$ to AD$_H$	Reserved				
AE$_H$	Flash Memory Control Status Register (Flash product only. Otherwise reserved)	FMCS	R/W	Flash Memory	0 0 0 X 0 0 0 0$_B$
AF$_H$	Reserved				

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Address	Register	Abbreviation	Access	Peripheral	Initial value
B0$_H$	Interrupt Control Register 00	ICR00	R/W	Interrupt controller	0 0 0 0 0 1 1 1$_B$
B1$_H$	Interrupt Control Register 01	ICR01	R/W		0 0 0 0 0 1 1 1$_B$
B2$_H$	Interrupt Control Register 02	ICR02	R/W		0 0 0 0 0 1 1 1$_B$
B3$_H$	Interrupt Control Register 03	ICR03	R/W		0 0 0 0 0 1 1 1$_B$
B4$_H$	Interrupt Control Register 04	ICR04	R/W		0 0 0 0 0 1 1 1$_B$
B5$_H$	Interrupt Control Register 05	ICR05	R/W		0 0 0 0 0 1 1 1$_B$
B6$_H$	Interrupt Control Register 06	ICR06	R/W		0 0 0 0 0 1 1 1$_B$
B7$_H$	Interrupt Control Register 07	ICR07	R/W		0 0 0 0 0 1 1 1$_B$
B8$_H$	Interrupt Control Register 08	ICR08	R/W		0 0 0 0 0 1 1 1$_B$
B9$_H$	Interrupt Control Register 09	ICR09	R/W		0 0 0 0 0 1 1 1$_B$
BA$_H$	Interrupt Control Register 10	ICR10	R/W		0 0 0 0 0 1 1 1$_B$
BB$_H$	Interrupt Control Register 11	ICR11	R/W		0 0 0 0 0 1 1 1$_B$
BC$_H$	Interrupt Control Register 12	ICR12	R/W		0 0 0 0 0 1 1 1$_B$
BD$_H$	Interrupt Control Register 13	ICR13	R/W		0 0 0 0 0 1 1 1$_B$
BE$_H$	Interrupt Control Register 14	ICR14	R/W		0 0 0 0 0 1 1 1$_B$
BF$_H$	Interrupt Control Register 15	ICR15	R/W		0 0 0 0 0 1 1 1$_B$
C0$_H$ to FF$_H$	Reserved				
1900$_H$	Reload L Register	PRLL0	R/W	16-bit Programmable Pulse Generator 0/1	XXXXXXXX$_B$
1901$_H$	Reload H Register	PRLH0	R/W		XXXXXXXX$_B$
1902$_H$	Reload L Register	PRLL1	R/W		XXXXXXXX$_B$
1903$_H$	Reload H Register	PRLH1	R/W		XXXXXXXX$_B$
1904$_H$	Reload L Register	PRLL2	R/W	16-bit Programmable Pulse Generator 2/3	XXXXXXXX$_B$
1905$_H$	Reload H Register	PRLH2	R/W		XXXXXXXX$_B$
1906$_H$	Reload L Register	PRLL3	R/W		XXXXXXXX$_B$
1907$_H$	Reload H Register	PRLH3	R/W		XXXXXXXX$_B$
1908$_H$	Reload L Register	PRLL4	R/W	16-bit Programmable Pulse Generator 4/5	XXXXXXXX$_B$
1909$_H$	Reload H Register	PRLH4	R/W		XXXXXXXX$_B$
190A$_H$	Reload L Register	PRLL5	R/W		XXXXXXXX$_B$
190B$_H$	Reload H Register	PRLH5	R/W		XXXXXXXX$_B$
190C$_H$	Reload L Register	PRLL6	R/W	16-bit Programmable Pulse Generator 6/7	XXXXXXXX$_B$
190D$_H$	Reload H Register	PRLH6	R/W		XXXXXXXX$_B$
190E$_H$	Reload L Register	PRLL7	R/W		XXXXXXXX$_B$
190F$_H$	Reload H Register	PRLH7	R/W		XXXXXXXX$_B$

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
1910$_H$	Reload L Register	PRLL8	R/W	16-bit Programmable Pulse Generator 8/9	XXXXXXXX$_B$
1911$_H$	Reload H Register	PRLH8	R/W		XXXXXXXX$_B$
1912$_H$	Reload L Register	PRLL9	R/W		XXXXXXXX$_B$
1913$_H$	Reload H Register	PRLH9	R/W		XXXXXXXX$_B$
1914$_H$	Reload L Register	PRLLA	R/W	16-bit Programmable Pulse Generator A/B	XXXXXXXX$_B$
1915$_H$	Reload H Register	PRLHA	R/W		XXXXXXXX$_B$
1916$_H$	Reload L Register	PRLLB	R/W		XXXXXXXX$_B$
1917$_H$	Reload H Register	PRLHB	R/W		XXXXXXXX$_B$
1918$_H$ to 191F$_H$	Reserved				
1920$_H$	Input Capture Register 0 (low-order)	IPCP0	R	Input Capture 0/1	XXXXXXXX$_B$
1921$_H$	Input Capture Register 0 (high-order)	IPCP0	R		XXXXXXXX$_B$
1922$_H$	Input Capture Register 1 (low-order)	IPCP1	R		XXXXXXXX$_B$
1923$_H$	Input Capture Register 1 (high-order)	IPCP1	R		XXXXXXXX$_B$
1924$_H$	Input Capture Register 2 (low-order)	IPCP2	R	Input Capture 2/3	XXXXXXXX$_B$
1925$_H$	Input Capture Register 2 (high-order)	IPCP2	R		XXXXXXXX$_B$
1926$_H$	Input Capture Register 3 (low-order)	IPCP3	R		XXXXXXXX$_B$
1927$_H$	Input Capture Register 3 (high-order)	IPCP3	R		XXXXXXXX$_B$
1928$_H$	Input Capture Register 4 (low-order)	IPCP4	R	Input Capture 4/5	XXXXXXXX$_B$
1929$_H$	Input Capture Register 4 (high-order)	IPCP4	R		XXXXXXXX$_B$
192A$_H$	Input Capture Register 5 (low-order)	IPCP5	R		XXXXXXXX$_B$
192B$_H$	Input Capture Register 5 (high-order)	IPCP5	R		XXXXXXXX$_B$
192C$_H$ to 192F$_H$	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
1930$_H$	Output Compare Register 0 (low-order)	OCCP0	R/W	Output Compare 0/1	XXXXXXXX$_B$
1931$_H$	Output Compare Register 0 (high-order)	OCCP0	R/W		XXXXXXXX$_B$
1932$_H$	Output Compare Register 1 (low-order)	OCCP1	R/W		XXXXXXXX$_B$
1933$_H$	Output Compare Register 1 (high-order)	OCCP1	R/W		XXXXXXXX$_B$
1934$_H$	Output Compare Register 2 (low-order)	OCCP2	R/W	Output Compare 2/3	XXXXXXXX$_B$
1935$_H$	Output Compare Register 2 (high-order)	OCCP2	R/W		XXXXXXXX$_B$
1936$_H$	Output Compare Register 3 (low-order)	OCCP3	R/W		XXXXXXXX$_B$
1937$_H$	Output Compare Register 3 (high-order)	OCCP3	R/W		XXXXXXXX$_B$
1938$_H$	Output Compare Register 4 (low-order)	OCCP4	R/W	Output Compare 4/5	XXXXXXXX$_B$
1939$_H$	Output Compare Register 4 (high-order)	OCCP4	R/W		XXXXXXXX$_B$
193A$_H$	Output Compare Register 5 (low-order)	OCCP5	R/W		XXXXXXXX$_B$
193B$_H$	Output Compare Register 5 (high-order)	OCCP5	R/W		XXXXXXXX$_B$
193C$_H$ to 193F$_H$	Reserved				
1940$_H$	Timer 0/Reload Register 0 (low-order)	TMR0/ TMRLR0	R/W	16-bit Reload Timer 0	XXXXXXXX$_B$
1941$_H$	Timer 0/Reload Register 0 (high-order)	TMR0/ TMRLR0	R/W		XXXXXXXX$_B$
1942$_H$	Timer 1/Reload Register 1 (low-order)	TMR1/ TMRLR1	R/W	16-bit Reload Timer 1	XXXXXXXX$_B$
1943$_H$	Timer 1/Reload Register 1 (high-order)	TMR1/ TMRLR1	R/W		XXXXXXXX$_B$
1944$_H$	Timer Data Register (low-order)	TCDT	R/W	16-bit Free-run Timer	00000000$_B$
1945$_H$	Timer Data Register (high-order)	TCDT	R/W		00000000$_B$
1946$_H$	Frequency Data Register	SGFR	R/W	Sound Generator	XXXXXXXX$_B$
1947$_H$	Amplitude Data Register	SGAR	R/W		XXXXXXXX$_B$
1948$_H$	Decrement Grade Register	SGDR	R/W		XXXXXXXX$_B$
1949$_H$	Tone Count Register	SGTR	R/W		XXXXXXXX$_B$

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
194A$_H$	Sub-second Data Register (low-order)	WTBR	R/W	Watch Timer	XXXXXXXX$_B$
194B$_H$	Sub-second Data Register (middle-order)	WTBR	R/W		XXXXXXXX$_B$
194C$_H$	Sub-second Data Register (high-order)	WTBR	R/W		_ _ _ XXXXX$_B$
194D$_H$	Second Data Register	WTSR	R/W		_ _ 0 0 0 0 0 0$_B$
194E$_H$	Minute Data Register	WTMR	R/W	Watch Timer	_ _ 0 0 0 0 0 0$_B$
194F$_H$	Hour Data Register	WTHR	R/W		_ _ _ 0 0 0 0 0$_B$
1950$_H$	PWM1 Compare Register 0	PWC10	R/W	Stepping Motor Controller 0	XXXXXXXX$_B$
1951$_H$	PWM2 Compare Register 0	PWC20	R/W		XXXXXXXX$_B$
1952$_H$	PWM1 Select Register 0	PWS10	R/W		_ _ 0 0 0 0 0 0$_B$
1953$_H$	PWM2 Select Register 0	PWS20	R/W		_ 0 0 0 0 0 0 0$_B$
1954$_H$	PWM1 Compare Register 1	PWC11	R/W	Stepping Motor Controller 1	XXXXXXXX$_B$
1955$_H$	PWM2 Compare Register 1	PWC21	R/W		XXXXXXXX$_B$
1956$_H$	PWM1 Select Register 1	PWS11	R/W		_ _ 0 0 0 0 0 0$_B$
1957$_H$	PWM2 Select Register 1	PWS21	R/W		_ 0 0 0 0 0 0 0$_B$
1958$_H$	PWM1 Compare Register 2	PWC12	R/W	Stepping Motor Controller 2	XXXXXXXX$_B$
1959$_H$	PWM2 Compare Register 2	PWC22	R/W		XXXXXXXX$_B$
195A$_H$	PWM1 Select Register 2	PWS12	R/W		_ _ 0 0 0 0 0 0$_B$
195B$_H$	PWM2 Select Register 2	PWS22	R/W		_ 0 0 0 0 0 0 0$_B$
195C$_H$	PWM1 Compare Register 3	PWC13	R/W	Stepping Motor Controller 3	XXXXXXXX$_B$
195D$_H$	PWM2 Compare Register 3	PWC23	R/W		XXXXXXXX$_B$
195E$_H$	PWM1 Select Register 3	PWS13	R/W		_ _ 0 0 0 0 0 0$_B$
195F$_H$	PWM2 Select Register 3	PWS23	R/W		_ 0 0 0 0 0 0 0$_B$
1960$_H$ to 19FF$_H$	Reserved				
1A00$_H$ to 1AFF$_H$	CAN Interface 0. Refer to section about CAN Controller				
1B00$_H$ to 1BFF$_H$	CAN Interface 1. Refer to section about CAN Controller				
1C00$_H$ to 1CFF$_H$	CAN Interface 0. Refer to section about CAN Controller				
1D00$_H$ to 1DFF$_H$	CAN Interface 1. Refer to section about CAN Controller				
1E00$_H$ to 1EFF$_H$	Reserved				

(Continued)

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Address	Register	Abbreviation	Access	Peripheral	Initial value
1FF0$_H$	Program Address Detection Register 0 (low-order)	PADR0	R/W	Address Match Detection Function	XXXXXXXX $_B$
1FF1$_H$	Program Address Detection Register 0 (middle-order)	PADR0	R/W		XXXXXXXX $_B$
1FF2$_H$	Program Address Detection Register 0 (high-order)	PADR0	R/W		XXXXXXXX $_B$
1FF3$_H$	Program Address Detection Register 1 (low-order)	PADR1	R/W		XXXXXXXX $_B$
1FF4$_H$	Program Address Detection Register 1 (middle-order)	PADR1	R/W		XXXXXXXX $_B$
1FF5$_H$	Program Address Detection Register 1 (high-order)	PADR1	R/W		XXXXXXXX $_B$
1FF6$_H$ to 1FFF$_H$	Reserved				

Note : Initial value of "_" represents unused bit; "X" represents unknown value.
　　　Addresses in the rage 0000$_H$ to 00FF$_H$, which are not listed in the table, are reserved for the primary functions of the MCU. A read access to these reserved addresses results in reading "X", and any write access should not be performed.

■ CAN CONTROLLERS

The CAN controller has the following features : Conforms to CAN Specification Version 2.0 Part A and B
- Supports transmission/reception in standard frame and extended frame formats

• Supports transmission of data frames by receiving remote frames
• 16 transmitting/receiving message buffers
- 29-bit ID and 8-byte data

- Multi-level message buffer configuration

• Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as 1D acceptance mask
- Two acceptance mask registers in either standard frame format or extended frame formats

• Bit rate programmable from 10 Kbit/s to 2 Mbit/s (when input clock is at 16 MHz)

List of Control Registers

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
000070_H	000080_H	Message buffer valid register	BVALR	R/W	00000000 00000000$_B$
000071_H	000081_H				
000072_H	000082_H	Transmit request register	TREQR	R/W	00000000 00000000$_B$
000073_H	000083_H				
000074_H	000084_H	Transmit cancel register	TCANR	W	00000000 00000000$_B$
000075_H	000085_H				
000076_H	000086_H	Transmit complete register	TCR	R/W	00000000 00000000$_B$
000077_H	000087_H				
000078_H	000088_H	Receive complete register	RCR	R/W	00000000 00000000$_B$
000079_H	000089_H				
$00007A_H$	$00008A_H$	Remote request receiving register	RRTRR	R/W	00000000 00000000$_B$
$00007B_H$	$00008B_H$				
$00007C_H$	$00008C_H$	Receive overrun register	ROVRR	R/W	00000000 00000000$_B$
$00007D_H$	$00008D_H$				
$00007E_H$	$00008E_H$	Receive interrupt enable register	RIER	R/W	00000000 00000000$_B$
$00007F_H$	$00008F_H$				

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FUJITSU

(Continued)

List of Control Registers

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
001C00$_H$	001D00$_H$	Control status register	CSR	R/W, R	00---000 0----0-1$_B$
001C01$_H$	001D01$_H$				
001C02$_H$	001D02$_H$	Last event indicator register	LEIR	R/W	-------- 000-0000$_B$
001C03$_H$	001D03$_H$				
001C04$_H$	001D04$_H$	Receive/transmit error counter	RTEC	R	00000000 00000000$_B$
001C05$_H$	001D05$_H$				
001C06$_H$	001D06$_H$	Bit timing register	BTR	R/W	-1111111 11111111$_B$
001C07$_H$	001D07$_H$				
001C08$_H$	001D08$_H$	IDE register	IDER	R/W	XXXXXXXX XXXXXXXX$_B$
001C09$_H$	001D09$_H$				
001C0A$_H$	001D0A$_H$	Transmit RTR register	TRTRR	R/W	00000000 00000000$_B$
001C0B$_H$	001D0B$_H$				
001C0C$_H$	001D0C$_H$	Remote frame receive waiting register	RFWTR	R/W	XXXXXXXX XXXXXXXX$_B$
001C0D$_H$	001D0D$_H$				
001C0E$_H$	001D0E$_H$	Transmit interrupt enable register	TIER	R/W	00000000 00000000$_B$
001C0F$_H$	001D0F$_H$				
001C10$_H$	001D10$_H$	Acceptance mask select register	AMSR	R/W	XXXXXXXX XXXXXXXX$_B$
001C11$_H$	001D11$_H$				
001C12$_H$	001D12$_H$				XXXXXXXX XXXXXXXX$_B$
001C13$_H$	001D13$_H$				
001C14$_H$	001D14$_H$	Acceptance mask register 0	AMR0	R/W	XXXXXXXX XXXXXXXX$_B$
001C15$_H$	001D15$_H$				
001C16$_H$	001D16$_H$				XXXXX--- XXXXXXXX$_B$
001C17$_H$	001D17$_H$				
001C18$_H$	001D18$_H$	Acceptance mask register 1	AMR1	R/W	XXXXXXXX XXXXXXXX$_B$
001C19$_H$	001D19$_H$				
001C1A$_H$	001D1A$_H$				XXXXX--- XXXXXXXX$_B$
001C1B$_H$	001D1B$_H$				

FUJITSU

List of Message Buffers (ID Registers)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
001A20$_H$	001B20$_H$	ID register 0	IDR0	R/W	XXXXXXXX XXXXXXXX$_B$
001A21$_H$	001B21$_H$				
001A22$_H$	001B22$_H$				XXXXX--- XXXXXXXX$_B$
001A23$_H$	001B23$_H$				
001A24$_H$	001B24$_H$	ID register 1	IDR1	R/W	XXXXXXXX XXXXXXXX$_B$
001A25$_H$	001B25$_H$				
001A26$_H$	001B26$_H$				XXXXX--- XXXXXXXX$_B$
001A27$_H$	001B27$_H$				
001A28$_H$	001B28$_H$	ID register 2	IDR2	R/W	XXXXXXXX XXXXXXXX$_B$
001A29$_H$	001B29$_H$				
001A2A$_H$	001B2A$_H$				XXXXX--- XXXXXXXX$_B$
001A2B$_H$	001B2B$_H$				
001A2C$_H$	001B2C$_H$	ID register 3	IDR3	R/W	XXXXXXXX XXXXXXXX$_B$
001A2D$_H$	001B2D$_H$				
001A2E$_H$	001B2E$_H$				XXXXX--- XXXXXXXX$_B$
001A2F$_H$	001B2F$_H$				
001A30$_H$	001B30$_H$	ID register 4	IDR4	R/W	XXXXXXXX XXXXXXXX$_B$
001A31$_H$	001B31$_H$				
001A32$_H$	001B32$_H$				XXXXX--- XXXXXXXX$_B$
001A33$_H$	001B33$_H$				
001A34$_H$	001B34$_H$	ID register 5	IDR5	R/W	XXXXXXXX XXXXXXXX$_B$
001A35$_H$	001B35$_H$				
001A36$_H$	001B36$_H$				XXXXX--- XXXXXXXX$_B$
001A37$_H$	001B37$_H$				
001A38$_H$	001B38$_H$	ID register 6	IDR6	R/W	XXXXXXXX XXXXXXXX$_B$
001A39$_H$	001B39$_H$				
001A3A$_H$	001B3A$_H$				XXXXX--- XXXXXXXX$_B$
001A3B$_H$	001B3B$_H$				
001A3C$_H$	001B3C$_H$	ID register 7	IDR7	R/W	XXXXXXXX XXXXXXXX$_B$
001A3D$_H$	001B3D$_H$				
001A3E$_H$	001B3E$_H$				XXXXX--- XXXXXXXX$_B$
001A3F$_H$	001B3F$_H$				

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Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
001A40$_H$	001B40$_H$	ID register 8	IDR8	R/W	XXXXXXXX XXXXXXXX$_B$
001A41$_H$	001B41$_H$				
001A42$_H$	001B42$_H$				XXXXX--- XXXXXXXX$_B$
001A43F$_H$	001B43$_H$				
001A44$_H$	001B44$_H$	ID register 9	IDR9	R/W	XXXXXXXX XXXXXXXX$_B$
001A45$_H$	001B45$_H$				
001A46$_H$	001B46$_H$				XXXXX--- XXXXXXXX$_B$
001A47$_H$	001B47$_H$				
001A48$_H$	001B48$_H$	ID register 10	IDR10	R/W	XXXXXXXX XXXXXXXX$_B$
001A49$_H$	001B49$_H$				
001A4A$_H$	001B4A$_H$				XXXXX--- XXXXXXXX$_B$
001A4B$_H$	001B4B$_H$				
001A4C$_H$	001B4C$_H$	ID register 11	IDR11	R/W	XXXXXXXX XXXXXXXX$_B$
001A4D$_H$	001B4D$_H$				
001A4E$_H$	001B4E$_H$				XXXXX--- XXXXXXXX$_B$
001A4F$_H$	001B4F$_H$				
001A50$_H$	001B50$_H$	ID register 12	IDR12	R/W	XXXXXXXX XXXXXXXX$_B$
001A51$_H$	001B51$_H$				
001A52$_H$	001B52$_H$				XXXXX--- XXXXXXXX$_B$
001A53$_H$	001B53$_H$				
001A54$_H$	001B54$_H$	ID register 13	IDR13	R/W	XXXXXXXX XXXXXXXX$_B$
001A55$_H$	001B55$_H$				
001A56$_H$	001B56$_H$				XXXXX--- XXXXXXXX$_B$
001A57$_H$	001B57$_H$				
001A58$_H$	001B58$_H$	ID register 14	IDR14	R/W	XXXXXXXX XXXXXXXX$_B$
001A59$_H$	001B59$_H$				
001A5A$_H$	001B5A$_H$				XXXXX--- XXXXXXXX$_B$
001A5B$_H$	001B5B$_H$				
001A5C$_H$	001B5C$_H$	ID register 15	IDR15	R/W	XXXXXXXX XXXXXXXX$_B$
001A5D$_H$	001B5D$_H$				
001A5E$_H$	001B5E$_H$				XXXXX--- XXXXXXXX$_B$
001A5F$_H$	001B5F$_H$				

List of Message Buffers (DLC Registers and Data Registers)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
001A60H	001B60H	DLC register 0	DLCR0	R/W	----XXXXB
001A61H	001B61H				
001A62H	001B62H	DLC register 1	DLCR1	R/W	----XXXXB
001A63H	001B63H				
001A64H	001B64H	DLC register 2	DLCR2	R/W	----XXXXB
001A65H	001B65H				
001A66H	001B66H	DLC register 3	DLCR3	R/W	----XXXXB
001A67H	001B67H				
001A68H	001B68H	DLC register 4	DLCR4	R/W	----XXXXB
001A69H	001B69H				
001A6AH	001B6AH	DLC register 5	DLCR5	R/W	----XXXXB
001A6BH	001B6BH				
001A6CH	001B6CH	DLC register 6	DLCR6	R/W	----XXXXB
001A6DH	001B6DH				
001A6EH	001B6EH	DLC register 7	DLCR7	R/W	----XXXXB
001A6FH	001B6FH				
001A70H	001B70H	DLC register 8	DLCR8	R/W	----XXXX
001A71H	001B71H				
001A72H	001B72H	DLC register 9	DLCR9	R/W	----XXXXB
001A73H	001B73H				
001A74H	001B74H	DLC register 10	DLCR10	R/W	----XXXXB
001A75H	001B75H				
001A76H	001B76H	DLC register 11	DLCR11	R/W	----XXXXB
001A77H	001B77H				
001A78H	001B78H	DLC register 12	DLCR12	R/W	----XXXXB
001A79H	001B79H				
001A7AH	001B7AH	DLC register 13	DLCR13	R/W	----XXXXB
001A7BH	001B7BH				
001A7CH	001B7CH	DLC register 14	DLCR14	R/W	----XXXXB
001A7DH	001B7DH				
001A7EH	001B7EH	DLC register 15	DLCR15	R/W	----XXXXB
001A7FH	001B7FH				
001A80H to 001A87H	001B80H to 001B87H	Data register 0 (8 bytes)	DTR0	R/W	XXXXXXXXB to XXXXXXXXB

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Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
$001A88_H$ to $001A8F_H$	$001B88_H$ to $001B8F_H$	Data register 1 (8 bytes)	DTR1	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$001A90_H$ to $001A97_H$	$001B90_H$ to $001B97_H$	Data register 2 (8 bytes)	DTR2	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$001A98_H$ to $001A9F_H$	$001B98_H$ to $001B9F_H$	Data register 3 (8 bytes)	DTR3	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$001AA0_H$ to $001AA7_H$	$001BA0_H$ to $001BA7_H$	Data register 4 (8 bytes)	DTR4	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$001AA8_H$ to $001AAF_H$	$001BA8_H$ to $001BAF_H$	Data register 5 (8 bytes)	DTR5	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$001AB0_H$ to $001AB7_H$	$001BB0_H$ to $001BB7_H$	Data register 6 (8 bytes)	DTR6	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$001AB8_H$ to $001ABF_H$	$001BB8_H$ to $001BBF_H$	Data register 7 (8 bytes)	DTR7	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$001AC0_H$ to $001AC7_H$	$001BC0_H$ to $001BC7_H$	Data register 8 (8 bytes)	DTR8	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$001AC8_H$ to $001ACF_H$	$001BC8_H$ to $001BCF_H$	Data register 9 (8 bytes)	DTR9	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$001AD0_H$ to $001AD7_H$	$001BD0_H$ to $001BD7_H$	Data register 10 (8 bytes)	DTR10	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$001AD8_H$ to $001ADF_H$	$001BD8_H$ to $001BDF_H$	Data register 11 (8 bytes)	DTR11	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$001AE0_H$ to $001AE7_H$	$001BE0_H$ to $001BE7_H$	Data register 12 (8 bytes)	DTR12	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$001AE8_H$ to $001AEF_H$	$001BE8_H$ to $001BEF_H$	Data register 13 (8 bytes)	DTR13	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$001AF0_H$ to $001AF7_H$	$001BF0_H$ to $001BF7_H$	Data register 14 (8 bytes)	DTR14	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$001AF8_H$ to $001AFF_H$	$001BF8_H$ to $001BFF_H$	Data register 15 (8 bytes)	DTR15	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$

■ INTERRUPT MAP

Interrupt cause	EI²OS clear	Interrupt vector		Interrupt control register	
		Number	Address	Number	Address
Reset	N/A	# 08	FFFFDC$_H$	—	—
INT9 instruction	N/A	# 09	FFFFD8$_H$	—	—
Exception	N/A	# 10	FFFFD4$_H$	—	—
Time Base Timer	N/A	# 11	FFFFD0$_H$	ICR00	0000B0$_H$
External Interrupt (INT0 to INT7)	*1	# 12	FFFFCC$_H$		
CAN 0 RX	N/A	# 13	FFFFC8$_H$	ICR01	0000B1$_H$
CAN 0 TX/NS	N/A	# 14	FFFFC4$_H$		
CAN 1 RX	N/A	# 15	FFFFC0$_H$	ICR02	0000B2$_H$
CAN 1 TX/NS	N/A	# 16	FFFFBC$_H$		
8/16 bit PPG 0/1	N/A	# 17	FFFFB8$_H$	ICR03	0000B3$_H$
8/16 bit PPG 2/3	N/A	# 18	FFFFB4$_H$		
8/16 bit PPG 4/5	N/A	# 19	FFFFB0$_H$	ICR04	0000B4$_H$
8/16 bit PPG 6/7	N/A	# 20	FFFFAC$_H$		
8/16 bit PPG 8/9	N/A	# 21	FFFFA8$_H$	ICR05	0000B5$_H$
8/16 bit PPG A/B	N/A	# 22	FFFFA4$_H$		
16-bit Reload Timer 0	*1	# 23	FFFFA0$_H$	ICR06	0000B6$_H$
16-bit Reload Timer 1	*1	# 24	FFFF9C$_H$		
Input Capture 0/1	*1	# 25	FFFF98$_H$	ICR07	0000B7$_H$
Output compare 0/1	*1	# 26	FFFF94$_H$		
Input Capture 2/3	*1	# 27	FFFF90$_H$	ICR08	0000B8$_H$
Output Compare 2/3	*1	# 28	FFFF8C$_H$		
Input Capture 4/5	*1	# 29	FFFF88$_H$	ICR09	0000B9$_H$
Output Compare 4/5	*1	# 30	FFFF84$_H$		
8/10 bit A/D Converter	*1	# 31	FFFF80$_H$	ICR10	0000BA$_H$
16-bit Free-run Timer/Watch Timer	N/A	# 32	FFFF7C$_H$		
Serial I/O	*1	# 33	FFFF78$_H$	ICR11	0000BB$_H$
Sound Generator	N/A	# 34	FFFF74$_H$		
UART 0 RX	*2	# 35	FFFF70$_H$	ICR12	0000BC$_H$
UART 0 TX	*1	# 36	FFFF6C$_H$		
UART 1 RX	*2	# 37	FFFF68$_H$	ICR13	0000BD$_H$
UART 1 TX	*1	# 38	FFFF64$_H$		
UART 2 RX	*2	# 39	FFFF60$_H$	ICR14	0000BE$_H$
UART 2 TX	*1	# 40	FFFF5C$_H$		
Flash Memory	N/A	# 41	FFFF58$_H$	ICR15	0000BF$_H$
Delayed interrupt	N/A	# 42	FFFF54$_H$		

*1 : The interrupt request flag is cleared by the EI^{2}OS interrupt clear signal.

*2 : The interrupt request flag is cleared by the EI^{2}OS interrupt clear signal. A stop request is available.

N/A : The interrupt request flag is not cleared by the EI^{2}OS interrupt clear signal.

Notes : • For a peripheral module with two interrupt for a single interrupt number, both interrupt request flags are cleared by the EI^{2}OS interrupt clear signal.
   • At the end of EI^{2}OS, the EI^{2}OS clear signal will be asserted for all the interrupt flags assigned to the same interrupt number. If one interrupt flag starts the EI^{2}OS and in the meantime another interrupt flag is set by a hardware event, the later event is lost because the flag is cleared by the EI^{2}OS clear signal caused by the first event. So it is recommended not to use the EI^{2}OS for this interrupt number.
   • If EI^{2}OS is enabled, EI^{2}OS is initiated when one of the two interrupt signals in the same interrupt control register (ICR) is asserted. This means that different interrupt sources share the same EI^{2}OS Descriptor which
   should be unique for each interrupt source. For this reason, when one interrupt source uses the EI^{2}OS, the other interrupt should be disabled.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

$(V_{SS} = AV_{SS} = 0.0 \text{ V})$

Parameter	Symbol	Rating Min	Rating Max	Unit	Remarks	
Power supply voltage	V_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V		
	AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_{CC} = AV_{CC}$	*1
	AVRH, AVRL	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$AV_{CC} \geq AVRH/L$, $AVRH \geq AVRL$	*1
	DV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_{CC} \geq DV_{CC}$	
Input voltage	V_I	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V		*2
Output voltage	V_O	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V		*2
Max clamp current	I_{CLAMP}	-2.0	$+2.0$	mA		*6
Total Max clamp current	$\sum | I_{CLAMP} |$	—	20	mA		*6
"L" level Max output current	I_{OL1}	—	15	mA	Normal output	*3
"L" level avg. output current	I_{OLAV1}	—	4	mA	Normal output, average value	*4
"L" level Max output current	I_{OL2}	—	40	mA	High current output	*3
"L" level avg. output current	I_{OLAV2}	—	30	mA	High current output, average value	*4
"L" level Max overall output current	$\sum I_{OL1}$	—	100	mA	Total normal output	
"L" level Max overall output current	$\sum I_{OL2}$		330	mA	Total high current output	
"L" level avg. overall output current	$\sum I_{OLAV1}$	—	50	mA	Total normal output, average value	*5
"L" level avg. overall output current	$\sum I_{OLAV2}$		250	mA	Total high current output, average value	*5
"H" level Max output current	I_{OH1}	—	-15	mA	Normal output	*3
"H" level avg. output current	I_{OHAV1}	—	-4	mA	Normal output, average value	*4
"H" level Max output current	I_{OH2}	—	-40	mA	High current output	*3
"H" level avg. output current	I_{OHAV2}	—	-30	mA	High current output, average value	*4
"H" level Max overall output current	$\sum I_{OH1}$	—	-100	mA	Total normal output	
"H" level Max overall output current	$\sum I_{OH2}$	—	-330	mA	Total high current output	
"H" level avg. overall output current	$\sum I_{OHAV1}$	—	-50	mA	Total normal output, average value	*5
"H" level avg. overall output current	$\sum I_{OHAV2}$	—	-250	mA	Total high current output, average value	*5
Power consumption	P_D	—	500	mW	MB90F594G, MB90F591G	
		—	400	mW	MB90594G, MB90591G	
Operating temperature	T_A	-40	$+85$	°C		
Storage temperature	T_{STG}	-55	$+150$	°C		

*1 : AV_{CC}, AVRH, AVRL and DV_{CC} shall not exceed V_{CC}. AVRH and AVRL shall not exceed AV_{CC}.
Also, AVRL shall not exceed AVRH.

*2 : V_I and V_O should not exceed $V_{CC} + 0.3V$. V_I should not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

*3 : The maximum output current is a peak value for a corresponding pin.

*4 : Average output current is an average current value observed for a 100 ms period for a corresponding pin.

*5 : Total average current is an average current value observed for a 100 ms period for all corresponding pins.

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*6 : • Applicable to pins : P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 toP95
• Use within recommended operating conditions.
• Use at DC voltage (current)
• The +B signal should always be applied with a limiting resistance placed between the +B signal and the microcontroller.
• The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pins does not exceed rated values, either instantaneously or for prolonged periods.
• Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the Vcc pin, and this may affect other devices.
• Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
• Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
• Care must be taken not to leave the +B input pin open.
• Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal input.
• Sample recommended circuits

• Input/Output equivalent circuits
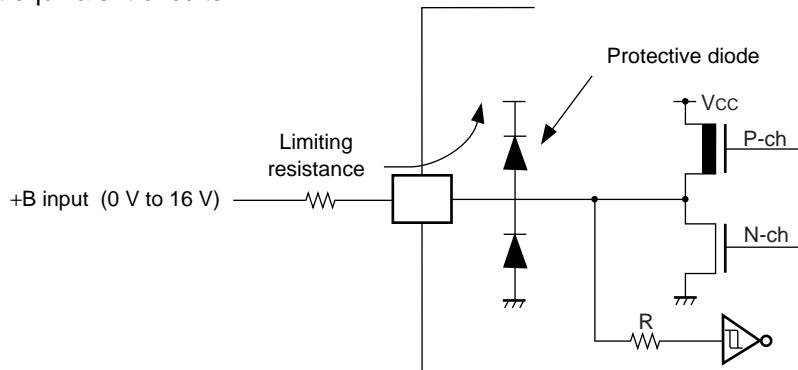
Note : Average output current = operating current × operating efficiency

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Conditions

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value			Unit	Remarks	
		Min	Typ	Max			
Power supply voltage	V_{CC} AV_{CC}	4.5	5.0	5.5	V	Under normal operation	MB90V590G MB90F594G MB90594G
		3.0	—	5.5	V	Maintains RAM data in stop mode	
		4.75	5.0	5.25	V	Under normal operation	MB90F591G MB90591G
		3.0	—	5.25	V	Maintains RAM data in stop mode	
Smooth capacitor	C_S	0.022	0.1	1.0	μF	*	
Operating temperature	T_A	–40	—	+85	°C		

* : Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The smoothing capacitor to be connected to the V_{CC} pin must have a capacitance value higher than C_S.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

• C Pin Connection Diagram
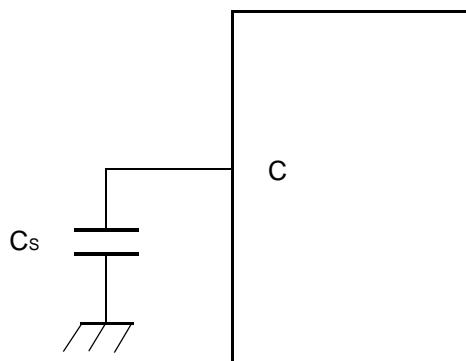
3. DC Characteristics

(MB90V590G, MB90F594G, MB90594G : V_{CC} = 5.0 V±10 %, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

(MB90F591G, MB90591G : V_{CC} = 5.0 V±5 %, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage	V_{IHS}	CMOS hysteresis input	—	0.8 V_{CC}	—	V_{CC} +0.3	V	
	V_{IHM}	MD input	—	V_{CC} – 0.3	—	V_{CC} +0.3	V	
Input L voltage	V_{ILS}	CMOS hysteresis input	—	V_{SS} – 0.3	—	0.5V_{CC}	V	
	V_{ILM}	MD input	—	V_{SS} – 0.3	—	V_{SS} + 0.3	V	
	V_{ILR}	$\overline{RST}$, $\overline{HST}$	—	V_{SS} – 0.3	—	0.2V_{CC}	V	
Output H voltage	V_{OH1}	Normal output	V_{CC} = 4.5 V, I_{OH1} = –4.0 mA	V_{CC} – 0.5	—	—	V	
	V_{OH2}	High current output	V_{CC} = 4.5 V, I_{OH2} = –30.0 mA	V_{CC} – 0.5	—	—	V	
Output L voltage	V_{OL1}	Normal output	V_{CC} = 4.5 V, I_{OL1} = 4.0 mA	—	—	0.4	V	
	V_{OL2}	High current output	V_{CC} = 4.5 V, I_{OL2} = 30.0 mA	—	—	0.5	V	
Input leak current	I_{IL}	—	V_{CC} = 5.5 V, V_{SS} < V_I < V_{CC}	–5	—	5	µA	
Analog input leak current	I_{IAL}	AN0 to AN7	V_{CC} = 5.5 V, AV_{SS} < V_I < AV_{CC}	–1	—	1	µA	
Power supply current *	I_{CC}	V_{CC}	V_{CC} = 5.0 V±10%, Internal frequency : 16 MHz, At normal operation.	—	37	60	mA	MB90594G
				—	50	80	mA	MB90F594G
				—	50	80	mA	MB90F591G
				—	45	60	mA	MB90591G
	I_{CCS}		V_{CC} = 5.0 V±10%, Internal frequency : 16 MHz, At Sleep mode.	—	13	20	mA	MB90594G
				—	15	23	mA	MB90F594G
				—	15	23	mA	MB90F591G
				—	15	23	mA	MB90591G
	I_{CTS}		V_{CC} = 5.0 V±10%, Internal frequency : 2 MHz, At Timer mode	—	0.3	0.6	mA	MB90594G
				—	0.35	0.6	mA	MB90F594G
				—	0.35	0.6	mA	MB90F591G
				—	0.35	0.6	mA	MB90591G
	I_{CCH}		V_{CC} = 5.0 V±10%, At Stop mode, T_A = 25°C	—	5	20	µA	MB90594G
				—	5	20	µA	MB90F594G
				—	5	20	µA	MB90F591G
				—	5	20	µA	MB90591G

* : The power supply current testing conditions are when using the external clock.

(Continued)

(Continued)
(MB90V590G, MB90F594G, MB90594G : V_{CC} = 5.0 V±10 %, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)
(MB90F591G, MB90591G : V_{CC} = 5.0 V±5 %, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input capacity	C_{IN}	Other than C, AV_{CC}, AV_{SS}, AVRH, AVRL, $V_{CC,}$ $V_{SS,}$ DV_{CC}, DV_{SS}, P70 to P87	—	—	5	15	pF	
		P70 to P87	—	—	15	30	pF	
Pull-up resistance	R_{UP}	$\overline{RST}$	—	25	50	100	kΩ	
Pull-down resistance	R_{DOWN}	MD2	—	25	50	100	kΩ	

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4. AC Characteristics

(1) Clock Timing

(MB90V590G, MB90F594G, MB90594G : V_{CC} = 5.0 V±10 %, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)
(MB90F591G, MB90591G : V_{CC} = 5.0 V±5 %, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Oscillation frequency	f_C	X0, X1	3	—	16	MHz	
Oscillation cycle time	t_{CYL}	X0, X1	62.5	—	333	ns	
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Duty ratio is about 30 to 70%.
Input clock rise and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When using external clock
Machine clock frequency	f_{CP}	—	1.5	—	16	MHz	
Machine clock cycle time	t_{CP}	—	62.5	—	666	ns	
Flash read cycle time	t_{CYCFL}	—	—	2 t_{CP}	—	ns	When Flash is accessed by CPU

• **Clock Timing**
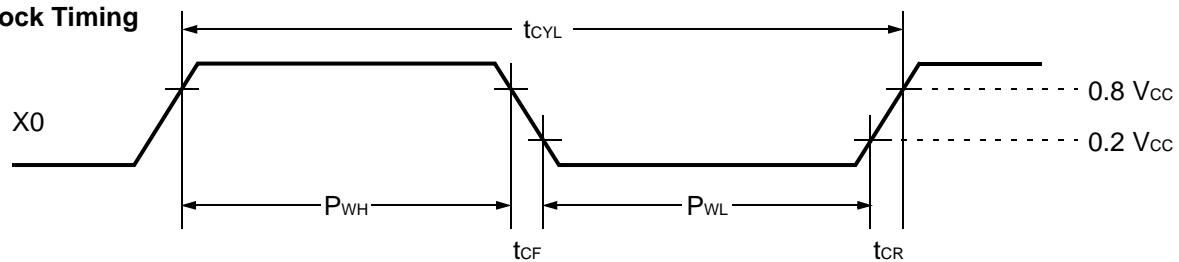
Example of Oscillation circuit

- **Guaranteed operation range**

Guaranteed operation range (MB90F591G, MB90591G)

Guaranteed operation range (MB90V590G, MB90F594G, MB90594G)

5.5
5.25
4.75
4.5

Power supply voltage
V_{CC} (V)

Guaranteed PLL operation range
(MB90F591G, MB90591G)

Guaranteed PLL operation range
(MB90V590G, MB90F594G, MB90594G)

3.0

1.5   8   16
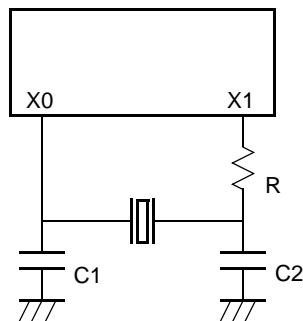
Machine clock f_{CP} (MHz)
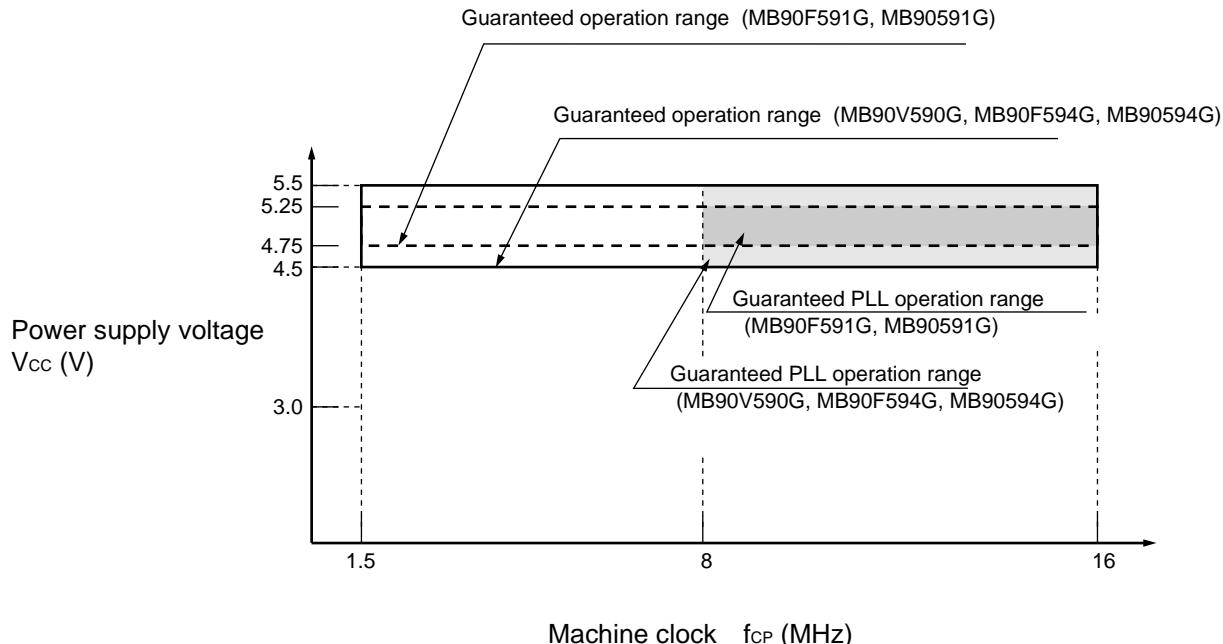
- **Oscillation clock frequency and machine clock frequency**

×4   ×3   ×2   ×1

16

12

Machine clock
f_{CP} (MHz)

9
8

×1/2
(PLL off)

4

3   4   8   16

Oscillation frequency f_C (MHz)

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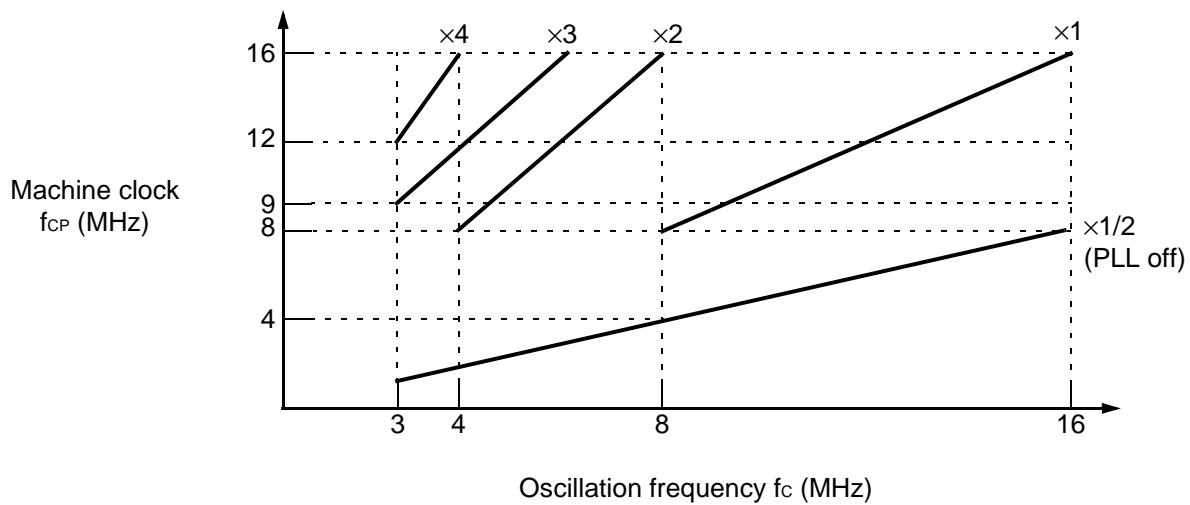
(2) Reset and Hardware Standby Input Timing

(MB90V590G, MB90F594G, MB90594G : V_{CC} = 5.0 V±10 %, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

(MB90F591G, MB90591G : V_{CC} = 5.0 V±5 %, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	16 t_{CP}*1	—	ns	Under normal operation
			Oscillation time of oscillator*2 + 16 t_{CP}*1	—	ms	In stop mode
Hardware standby input time	t_{HSTL}	$\overline{HST}$	16 t_{CP}*1	—	ns	Under normal operation

*1 : "t_{cp}" represents one cycle time of the machine clock.
No reset can fully initialize the Flash Memory if it is performing the automatic algorithm.

*2 : Oscillation time of oscillator is time that the amplitude reached the 90%.
In the crystal oscillator, the oscillation time is between several ms to tens of ms. In ceramic oscillator, the oscillation time is between hundreds of μs to several ms. In the external clock, the oscillation time is 0 ms.
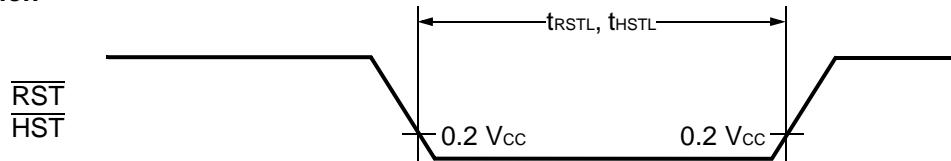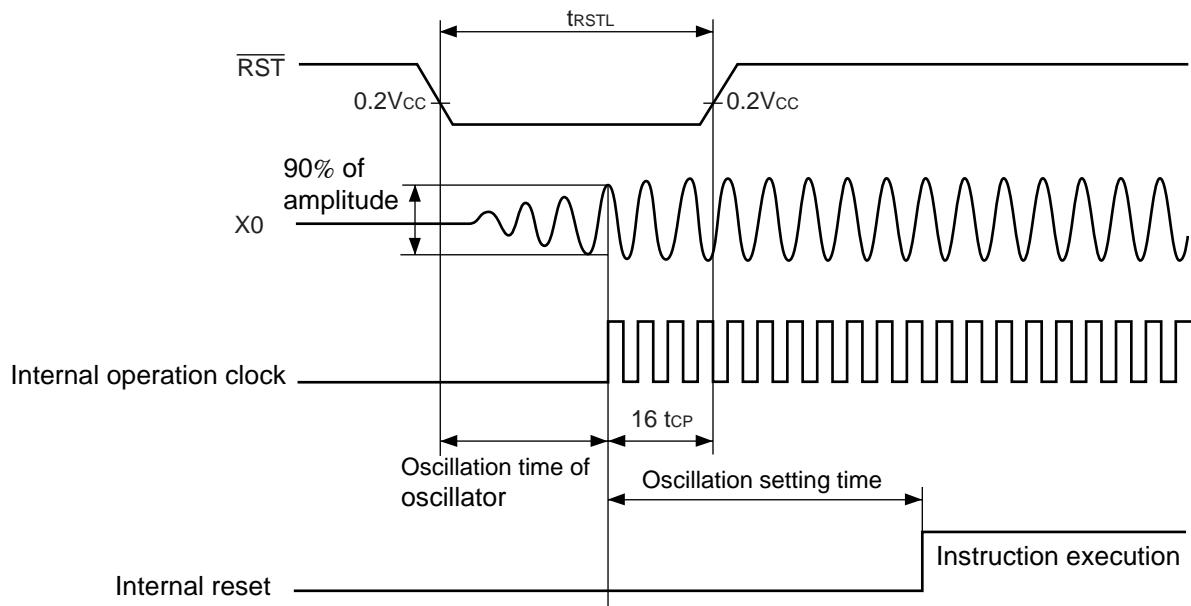
(3) Power On Reset

(MB90V590G, MB90F594G, MB90594G : V_{CC} = 5.0 V±10 %, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

(MB90F591G, MB90591G : V_{CC} = 5.0 V±5 %, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Power on rise time	t_R	V_{CC}	—	0.05	30	ms	
Power off time	t_{OFF}	V_{CC}		50	—	ms	Due to repetitive operation

Notes : • V_{CC} must be kept lower than 0.2 V before power-on.
   • The above values are used for creating a power-on reset.
   • Some registers in the device are initialized only upon a power-on reset. To initialize these register, turn on the power supply using the above values.

t_R

V_{CC}　　　　2.7 V

0.2 V　　　　　　　　　　0.2 V　　　0.2 V

t_{OFF}
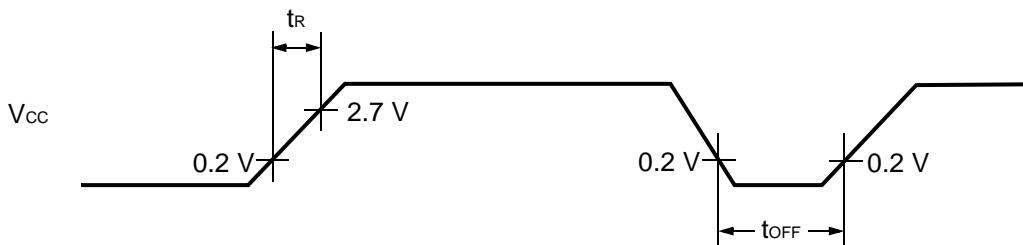
Sudden changes in the power supply voltage may cause a power-on reset.
To change the power supply voltage while the device is in operation, it is recommended to raise the voltage smoothly to suppress fluctuations as shown below.
In this case, change the supply voltage with the PLL clock not used. If the voltage drop is 1 V or fewer per second, however, you can use the PLL clock.

V_{CC}

3V

RAM data being held

V_{SS}

It is recommended to keep the rising speed of the supply voltage at 50 mV/ms or slower.
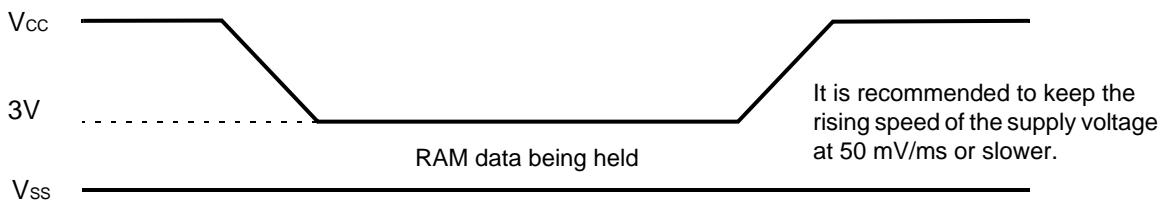
(4) UART0/1/2, Serial I/O Timing

(MB90V590G, MB90F594G, MB90594G : V_{CC} = 5.0 V±10 %, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

(MB90F591G, MB90591G : V_{CC} = 5.0 V±5 %, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal clock operation output pins are C_L = 80 pF + 1 TTL.	8 t_{CP}*	—	ns	
SCK ↓ ⇒ SOT delay time	t_{SLOV}	SCK0 to SCK3, SOT0 to SOT3		−80	80	ns	
Valid SIN ⇒ SCK ↑	t_{IVSH}	SCK0 to SCK3, SIN0 to SIN3		100	—	ns	
SCK ↑ ⇒ Valid SIN hold time	t_{SHIX}	SCK0 to SCK3, SIN0 to SIN3		60	—	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK3	External clock operation output pins are C_L = 80 pF + 1 TTL.	4 t_{CP}	—	ns	
Serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK3		4 t_{CP}	—	ns	
SCK ↓ ⇒ SOT delay time	t_{SLOV}	SCK0 to SCK3, SOT0 to SOT3		—	150	ns	
Valid SIN ⇒ SCK ↑	t_{IVSH}	SCK0 to SCK3, SIN0 to SIN3		60	—	ns	
SCK ↑ ⇒ Valid SIN hold time	t_{SHIX}	SCK0 to SCK3, SIN0 to SIN3		60	—	ns	

* : t_{CP} is the machine cycle (Unit : ns)

Notes : • AC characteristic in CLK synchronized mode.
  • C_L is load capacity value of pins when testing.

• **Internal Shift Clock Mode**
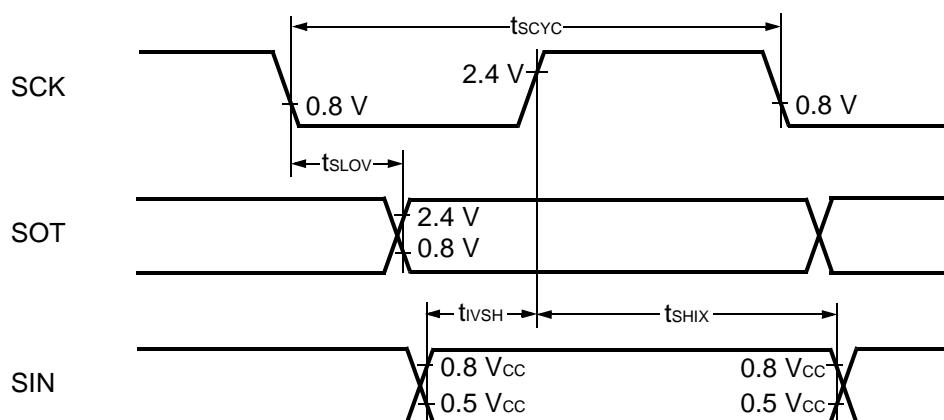
• **External Shift Clock Mode**

(5)Timer Input Timing

(MB90V590G, MB90F594G, MB90594G : V_{CC} = 5.0 V±10 %, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

(MB90F591G, MB90591G : V_{CC} = 5.0 V±5 %, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}	TIN0	—	4 t_{CP}	—	ns	Under normal operation
	t_{TIWL}	IN0 to IN5		1	—	µs	In stop mode

• **Timer Input Timing**

(6)Trigger Input Timing

(MB90V590G, MB90F594G, MB90594G : V_{CC} = 5.0 V±10 %, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

(MB90F591G, MB90591G : V_{CC} = 5.0 V±5 %, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH} t_{TRGL}	INT0 to INT7, ADTG	—	5 t_{CP}	—	ns	

• **Trigger Input Timing**
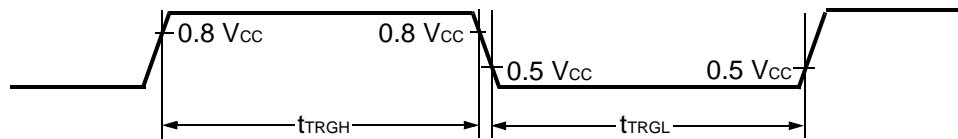
(7) Slew Rate High Current Outputs (MB90F591G, MB90591G, MB90594G and MB90F594G only)

(MB90F594G, MB90594G : V_{CC} = 5.0 V±10 %, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

(MB90F591G, MB90591G : V_{CC} = 5.0 V±5 %, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Output Rise/Fall time	t_{R2} t_{F2}	Port P70 to P77, Port P80 to P87	—	15	40	ns	

• Slew Rate Output Timing

$$V_H = V_{OL2} + 0.1 \times (V_{OH2} - V_{OL2})$$
$$V_L = V_{OL2} + 0.9 \times (V_{OH2} - V_{OL2})$$
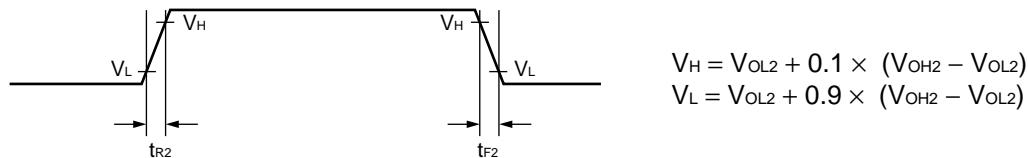
5. A/D Converter

(MB90V590G, MB90F594G, MB90594G :

$V_{CC} = AV_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $3.0 \text{ V} \leq AVR+ - AVR\text{-}$, $T_A = -40\,°C \text{ to } +85\,°C$)

(MB90F591G, MB90591G :

$V_{CC} = AV_{CC} = 5.0 \text{ V} \pm 5\%$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $3.0 \text{ V} \leq AVR+ - AVR\text{-}$, $T_A = -40\,°C \text{ to } +85\,°C$)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Conversion error	—	—	—	—	±5.0	LSB	
Nonlinearity error	—	—	—	—	±2.5	LSB	
Differential linearity error	—	—	—	—	±1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	AVRL − 3.5 LSB	AVRL + 0.5 LSB	AVRL + 4.5 LSB	V	
Full scale transition voltage	V_{FST}	AN0 to AN7	AVRH − 6.5 LSB	AVRH − 1.5 LSB	AVRH + 1.5 LSB	V	
Compare time	—	—	$352t_{CP}$	—	—	ns	Internal frequency : 16 MHz
Sampling time	—	—	$64t_{CP}$	—	—	ns	Internal frequency : 16 MHz
Analog port input current	I_{AIN}	AN0 to AN7	-1	—	+1	µA	
Analog input voltage range	V_{AIN}	AN0 to AN7	AVRL	—	AVRH	V	
Reference voltage range	—	AVRH	AVRL + 2.7	—	AV_{CC}	V	
	—	AVRL	0	—	AVRH − 2.7	V	
Power supply current	I_A	AV_{CC}	—	5	—	mA	
	I_{AH}	AV_{CC}	—	—	5	µA	*
Reference voltage current	I_R	AVRH	—	400	600	µA	MB90V590G MB90F594G MB90F591G
			—	140	600	µA	MB90594G MB90591G
	I_{RH}	AVRH	—	—	5	µA	*
Offset between input channels	—	AN0 to AN7	—	—	4	LSB	

* : When not operating A/D converter, this is the current ($V_{CC} = AV_{CC} = AVRH = 5.0 \text{ V}$) when the CPU is stopped.

6.   A/D Converter Glossary

Resolution : Analog changes that are identifiable with the A/D converter

Linearity error : The deviation of the straight line connecting the zero transition point ("00 0000 0000" $\leftrightarrow$ "00 0000 0001") with the full-scale transition point ("11 1111 1110" $\leftrightarrow$ "11 1111 1111") from actual conversion characteristics

Differential linearity error : The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value

Total error : The total error is defined as a difference between the actual value and the theoretical value, which includes zero-transition error/full-scale transition error and linearity error.
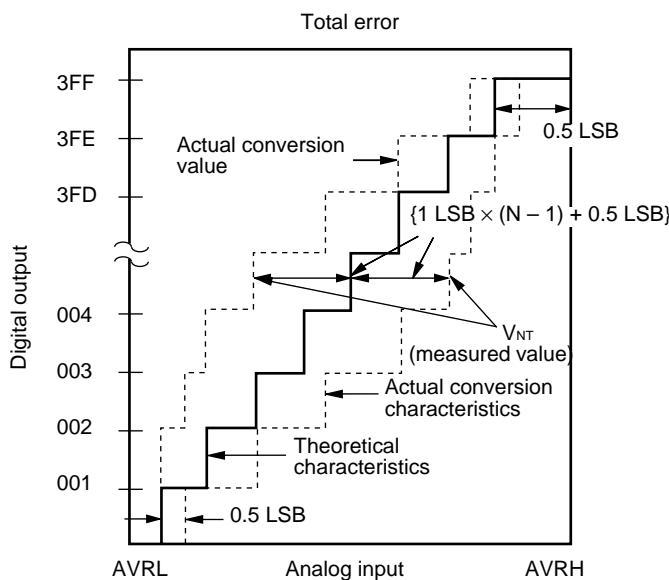
$$1\ \text{LSB} = (\text{Theoretical value})\ \frac{\text{AVRH} - \text{AVRL}}{1024}\ [V]$$

V_{OT} (Theoretical value) = AVRL + 0.5 LSB[V]

V_{FST} (Theoretical value) = AVRH – 1.5 LSB[V]

$$\text{Total error for digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

V_{NT} : Voltage at a transition of digital output from (N – 1) to N

(Continued)

(Continued)

Linearity error

$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\text{ LSB} \times (N - 1) + V_{OT}\}}{1\text{ LSB}} \text{ [LSB]}$$

$$\text{Differential linearity error of digital N} = \frac{V_{(N + 1)T} - V_{NT}}{1\text{ LSB}} - 1\text{ LSB [LSB]}$$

$$1\text{ LSB} = \frac{V_{FST} - V_{OT}}{1022} \text{ [V]}$$

V_{OT} : Voltage at transition of digital output from "000$_H$" to "001$_H$"
V_{FST} : Voltage at transition of digital output from "3FE$_H$" to "3FF$_H$"
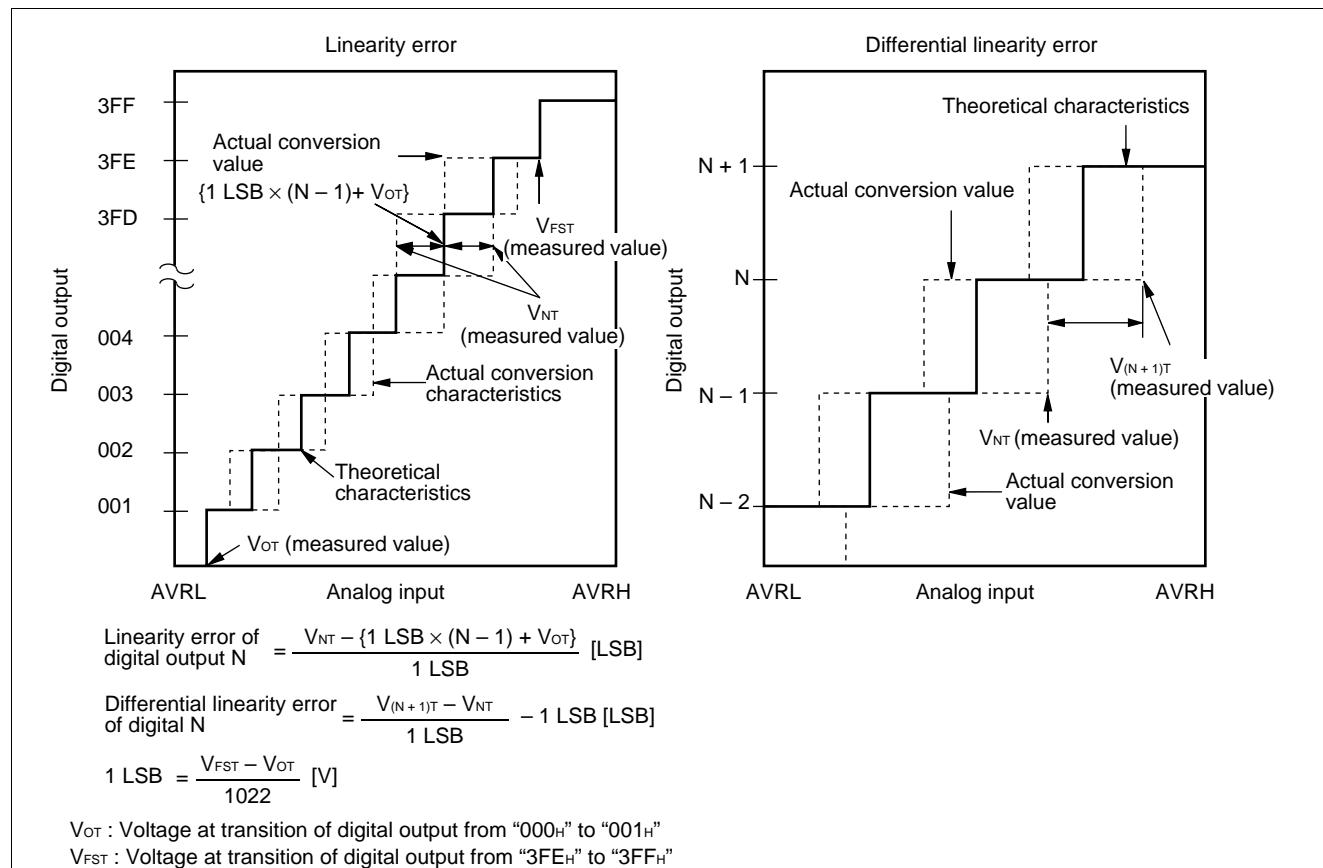
7. Notes on Using A/D Converter

Select the output impedance value for the external circuit of analog input according to the following conditions, :
- Output impedance values of the external circuit of 15 kΩ or lower are recommended.
- When capacitors are connected to external pins, the capacitance of several thousand times the internal capacitor value is recommended to minimized the effect of voltage distribution between the external capacitor and internal capacitor.

When the output impedance of the external circuit is too high, the sampling period for analog voltages may not be sufficient (sampling period = 4.00 μs @machine clock of 16 MHz).

- **Equipment of analog input circuit model**
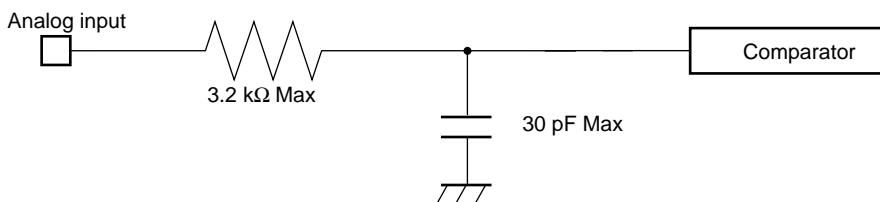
Note : Listed values must be considered as standards.

- **Error**

The smaller the | AVRH − AVRL |, the greater the error would become relatively.

8. Flash Memory

• Erase and Programming Performance

Parameter	Condition	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	$T_A = +25\ °C$ $V_{CC} = 5.0\ V$	—	1	15	s	Excludes 00H programming prior erasure
Chip erase time		—	7	—	s	MB90F594G — Excludes 00H programming prior erasure
		—	12	—	s	MB90F591G — Excludes 00H programming prior erasure
Word (16-bit) programming time		—	16	3,600	ns	Excludes system-level overhead
Erase/Program cycle	—	10,000	—	—	cycle	

MB90590G Series

■ EXAMPLE CHARACTERISTICS

• "H" Level Output Voltage

$V_{OH1} - I_{OH1}$
(V_{CC} = 4.5 V, T_A = +25°C)

$V_{OH2} - I_{OH2}$
(V_{CC} = 4.5 V, T_A = +25°C)

• "L" Level Output Voltage

$V_{OL1} - I_{OL1}$
(V_{CC} = 4.5 V, T_A = +25°C)

$V_{OL2} - I_{OL2}$
(V_{CC} = 4.5 V, T_A = +25°C)
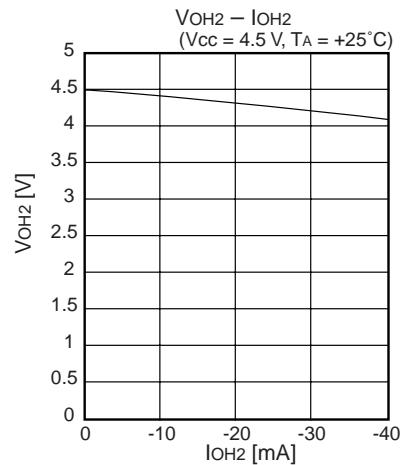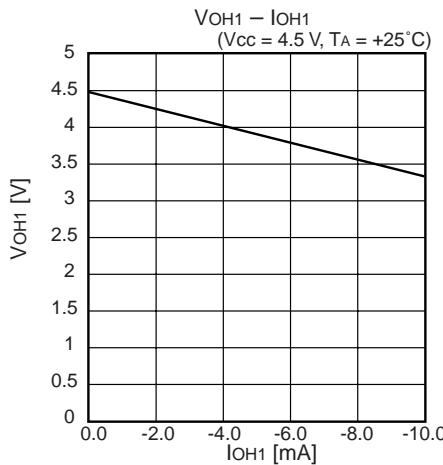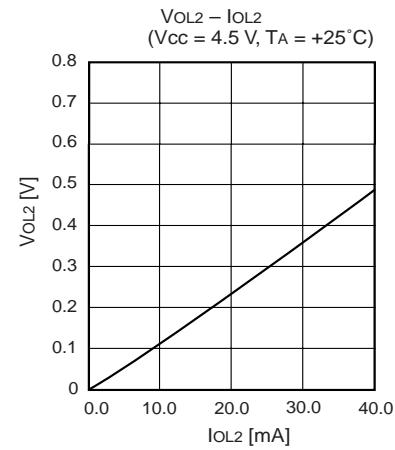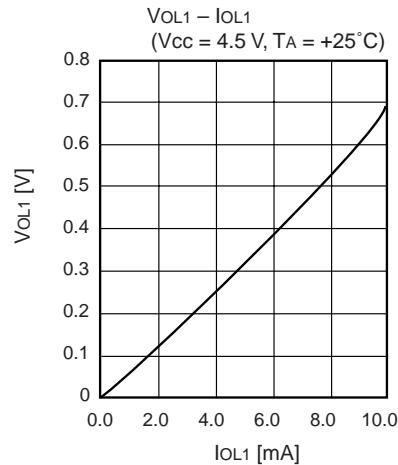
• "H" Level Input Voltage/"L Level Input Voltage (Hysteresis Input)

$V_{IN} - V_{CC}$
(T_A = +25°C)

V_{IH}

V_{IL}

(Continued)

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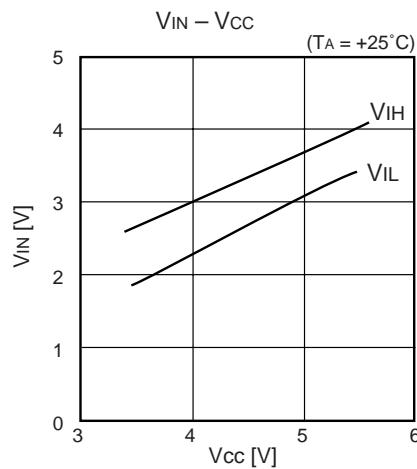
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• **Power Supply Voltage**

$I_{CC} - V_{CC}$
(T_A = +25˚C)

$I_{CCS} - V_{CC}$
(T_A = +25˚C)

$I_{CTS} - V_{CC}$
(T_A =˚C)

$I_{CCH} - V_{CC}$
(T_A =˚C)
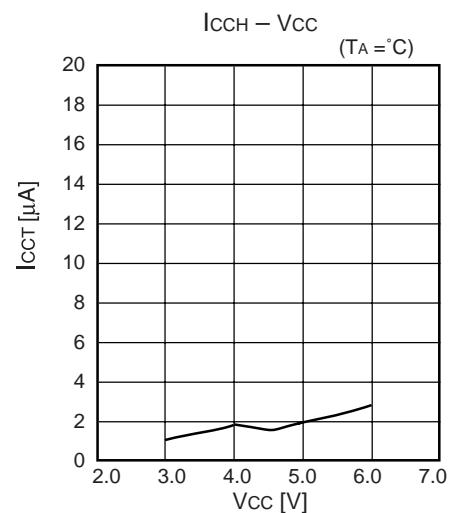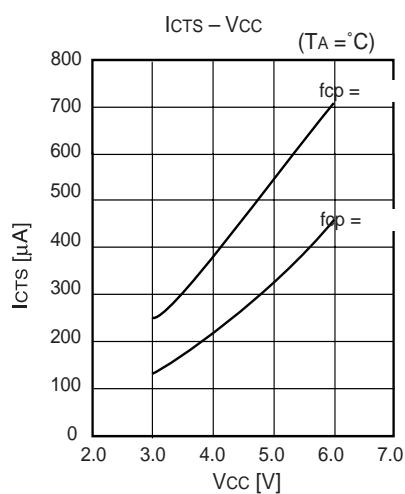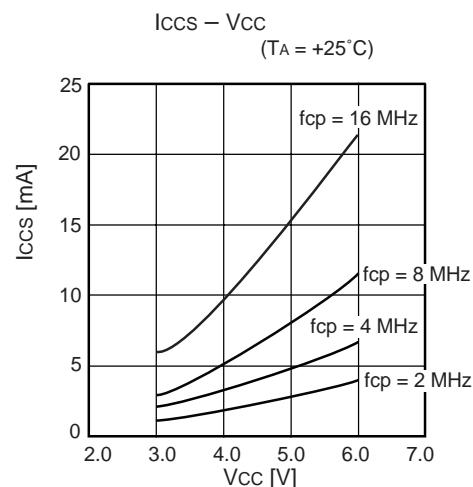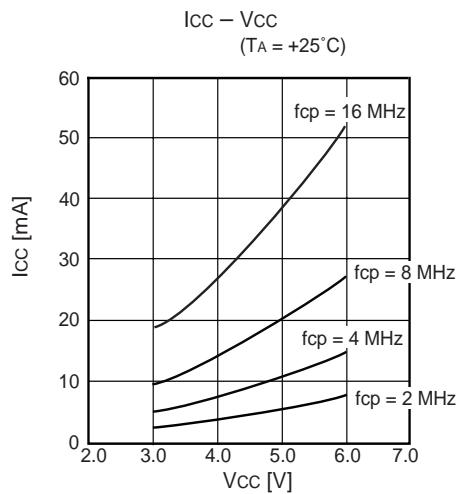
■ ORDERING INFORMATION

Part number	Package	Remarks
MB90594GPF MB90F594GPF MB90F591GPF MB90591GPF	100-pin Plastic QFP (FPT-100P-M06)	
MB90V590GCR	256-pin Ceramic PGA (PGA-256C-A01)	For evaluation

■ PACKAGE DIMENSION

100-pin plastic QFP	Lead pitch	0.65 mm
	Package width × package length	14.00 × 20.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	3.35 mm MAX
	Code (Reference)	P-QFP100-14×20-0.65
(FPT-100P-M06)		

100-pin plastic QFP
(FPT-100P-M06)

Note 1) ∗ : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.

23.90±0.40(.941±.016)
∗20.00±0.20(.787±.008)

80   51
81   50

0.10(.004)

17.90±0.40
(.705±.016)
∗14.00±0.20
(.551±.008)

INDEX

100   31

Details of "A" part

$3.00 ^{+0.35}_{-0.20}$
$(.118 ^{+.014}_{-.008})$
(Mounting height)

0.25(.010)

0~8°

1   30

0.65(.026)   0.32±0.05
(.013±.002)   ⊕ 0.13(.005) Ⓜ

0.17±0.06
(.007±.002)

0.80±0.20
(.031±.008)

0.25±0.20
(.010±.008)
(Stand off)

0.88±0.15
(.035±.006)

"A"

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Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
—	—	Deleted the part numbers. MB90591, MB90F591A, MB90594, MB90F594A, MB90V590A
—	—	Changed the series name. MB90590/590G series → MB90590G series
—	—	Changed the following name. I/O Timer → 16-bit Free-run Timer
—	—	Peripheral Resource name is changed. Clock Timer → Watch Timer
—	—	one of Standby mode name is changed. Clock mode → Watch mode
17	■ BLOCK DIAGRAM	Changed the number of channels of 16-bit output compare. 4 ch → 6 ch
35	■ INTERRUPT MAP	Changed the abbreviation of Extended Intelligent I/O Service. I²OS → EI²OS
48	■ ELECTRICAL CHARACTERISTICS 5. A/D Converter	Changed the items of "Zero transition voltage" and "Full scale transition voltage". mV → V

The vertical lines marked in the left side of the page show the changes.

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